# Ultra low power era
# Adding functionalities to CMOS

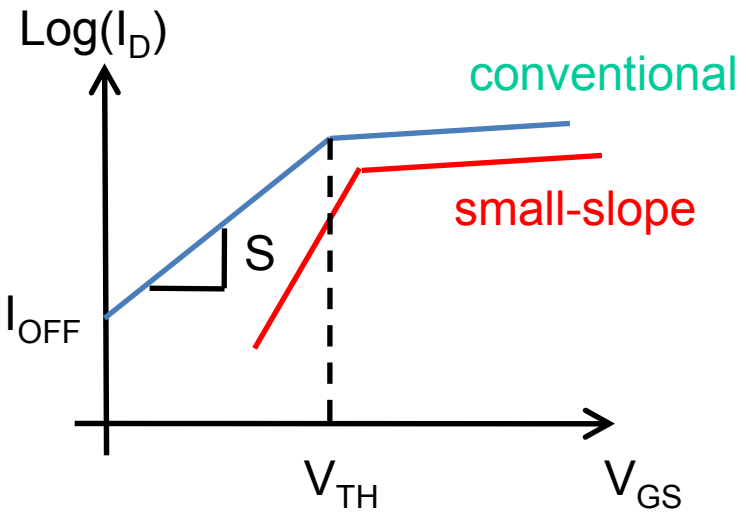
Enrico Sangiorgi

IU.NET – University of Bologna

***SiNANO INSTITUTE***

Sinano Institute, Grenoble INP-Minatec, 3 Parvis Louis Néel, BP 257, 38016 Grenoble-France Tel : +33 4 56 52 95 10 – Fax : +33 4 56 52 95 01 – Web : www.sinano.eu

# Ultra low power era -Small Slope Switches




- Conventional: $S \approx \ln(10) k_B T > 60\text{mV/dec@300K}$
- Advantages of small slope:
  - Same $V_{TH}$: lower $I_{OFF}$
  - Same $I_{OFF}$: lower $V_{TH}$ → lower $V_{DD}$

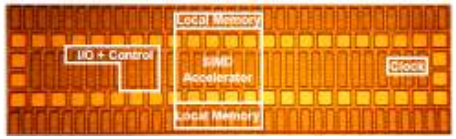
- Possible implementations:
  - Tunnel-FET
    - Bulk, DG-SOI Si FET
    - III-V materials
    - Graphene-based (?)
  - Ferroelectric materials in the gate stack
  - Junction-less FET
  - IMOS

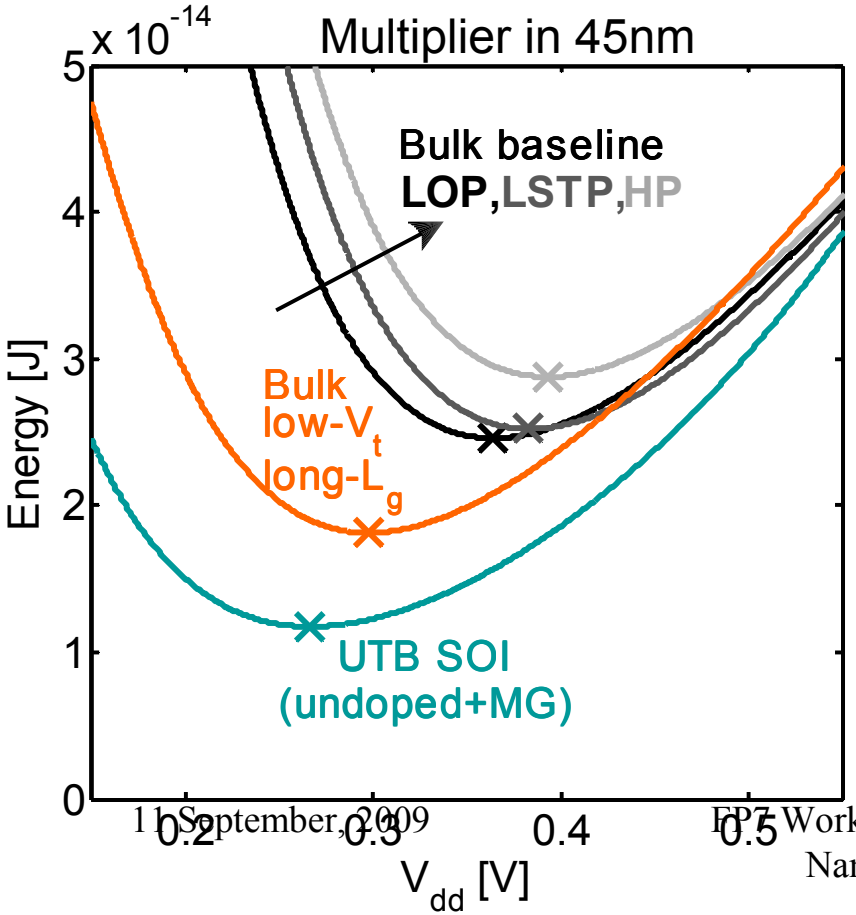
- State-of-the-art
  - Many T-FET structures proposed and fabricated so far, also in Europe
  - S<60mV/dec only over a small $V_{GS}$ range
  - Leakage currents may result in a fake S<60mV/dec

# Ultra-low-power circuits

**Fact:** nano-CMOS enables subthreshold design (ultra-low $V_{dd}$) for mid-perf. 1-100MHz applications [Bol,Trans. VLSI'09 EU]

**Example:** Intel 45nm SIMD coproc. [Kaul,ISSCC'09] minimum energy 33MHz @0.3V




**For minimizing energy:**
- new device paradigms (variability !)
- new device architecture

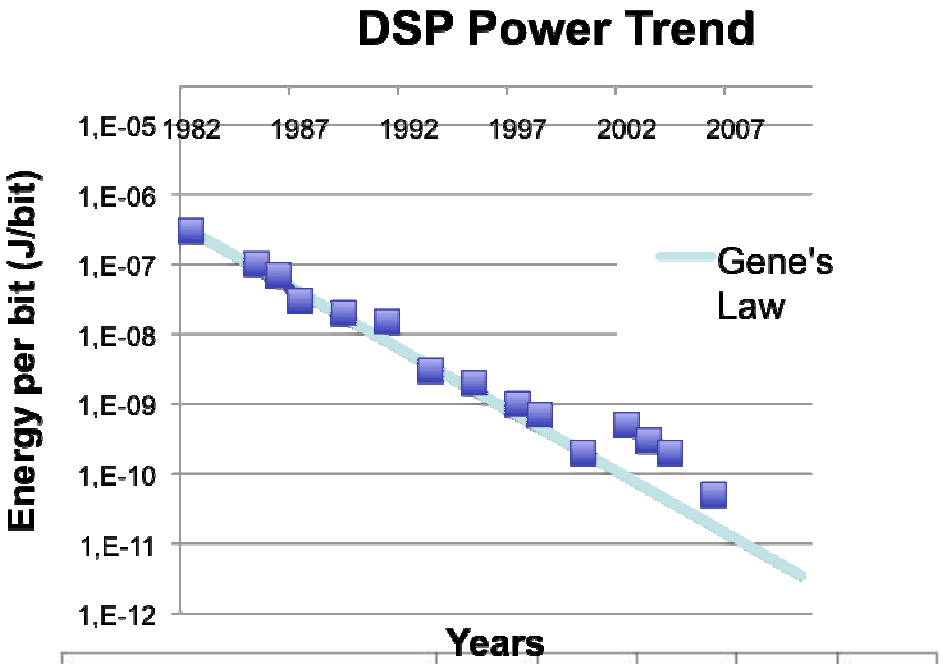
[Bol,ISLPED'09][Bol,SOIC'08] (EU)

**For SRAM robustness:**
- technology/circuit co-design (UTB SOI + BG biasing + 7-12T cell arch.) [Hu,TED'09][Verma,JSSC'08]

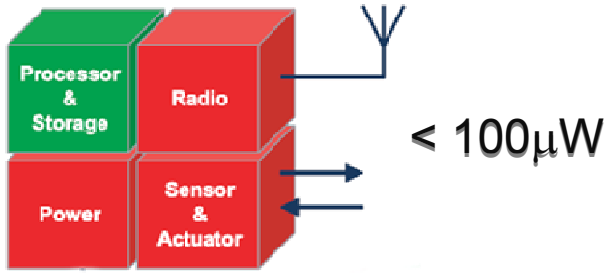
**For efficient design:**
- variability/PVT prediction+modeling
- tools for lognormal statistical design

# Ultra low power Systems: Energy Autonomous Systems

< 1cm³




| Year of production | 2008 | 2009 | 2012 | 2015 | 2018 |
|---|---|---|---|---|---|
| ADC power efficiency (pJ/S.) | 2 | 0.7 | 0.2 | 0.07 | 0.03 |



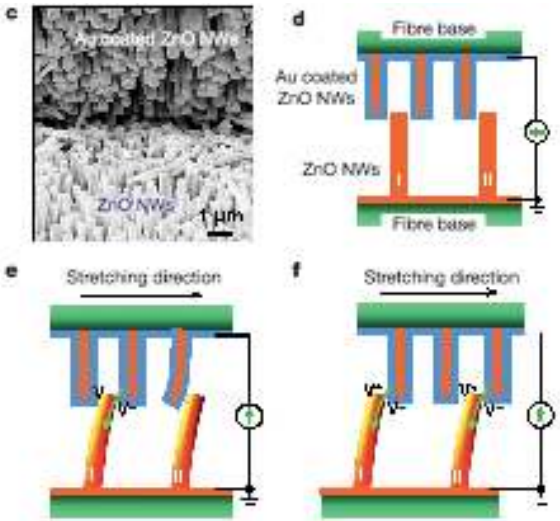

Ambient energy

Challenging
Perspective
Existing

**Source: M. Belleville, CATRENE Report on Energy Autonomous Systems EU**

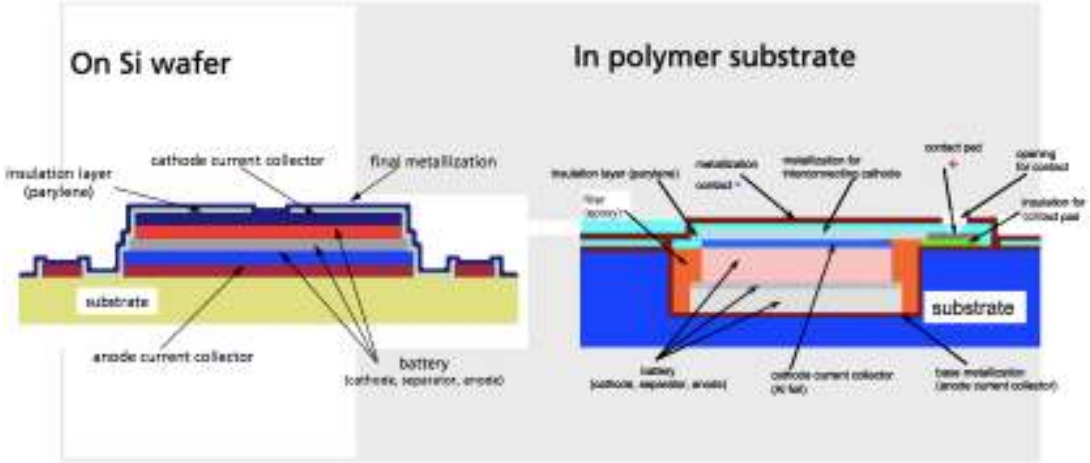
Tentative Roadmap

# Adding Energy Storage to CMOS

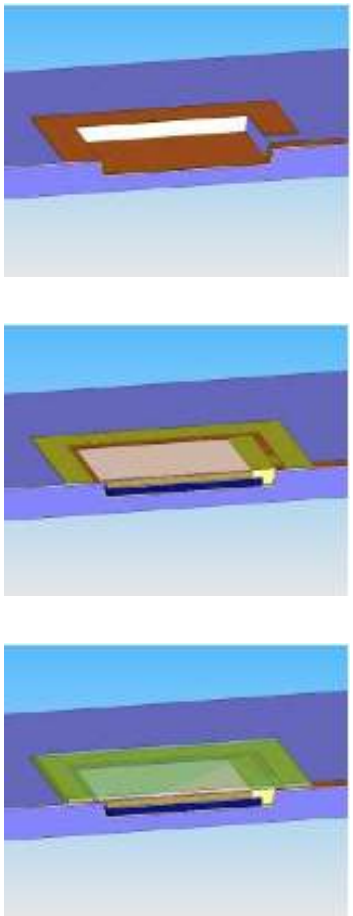



Nanopillars for Energy scavenging

Z. L. Wang, Nature, Vol.445, 809 (2008)

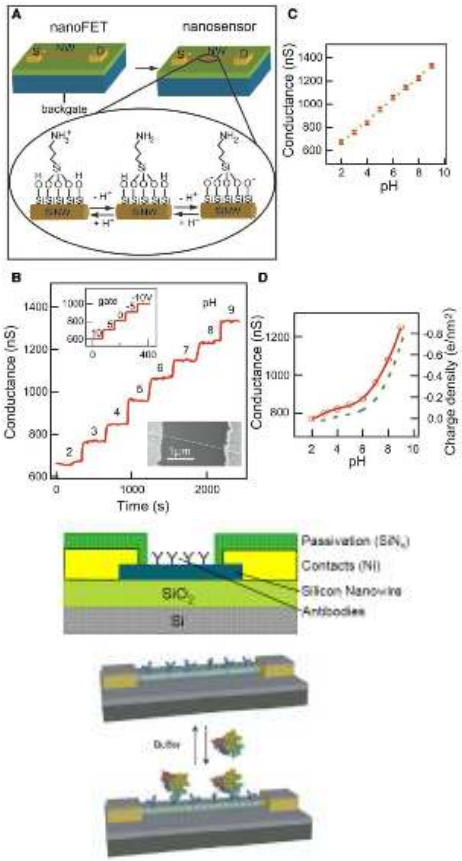



Microbatteries



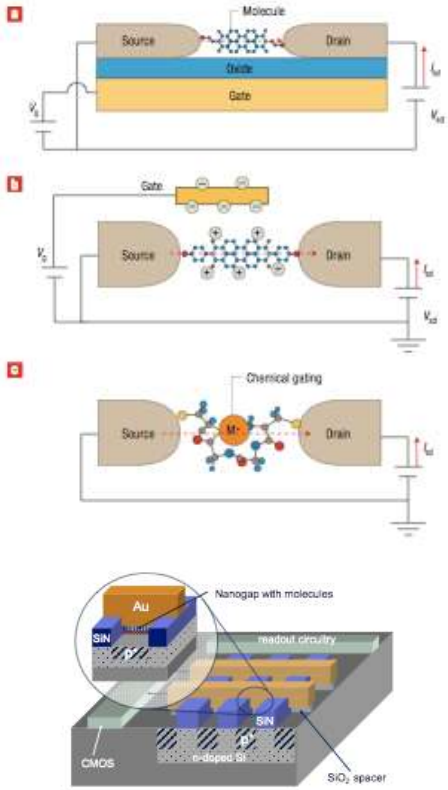
Source: R. Hahn, FhG, Berlin

# Adding Nanostructures to CMOS



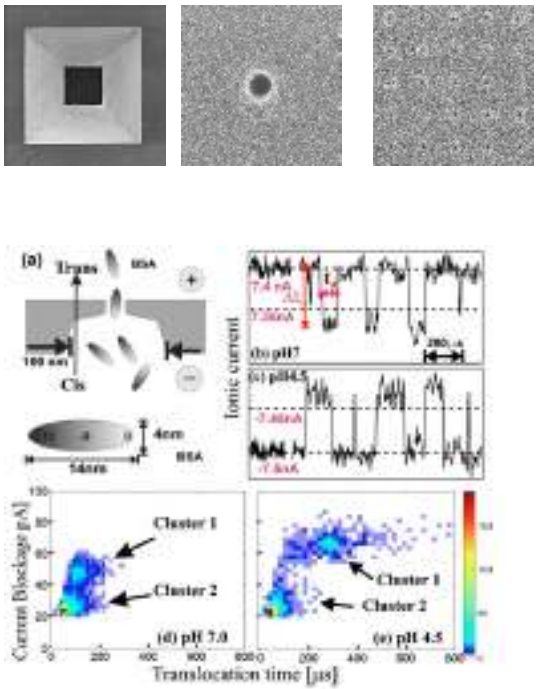

M. Reed, Nature, Vol.445, 1 (2007)

Nanowires




J. Tao, Nat. Nan. Vol.1, 173 (2006)

Nanogaps



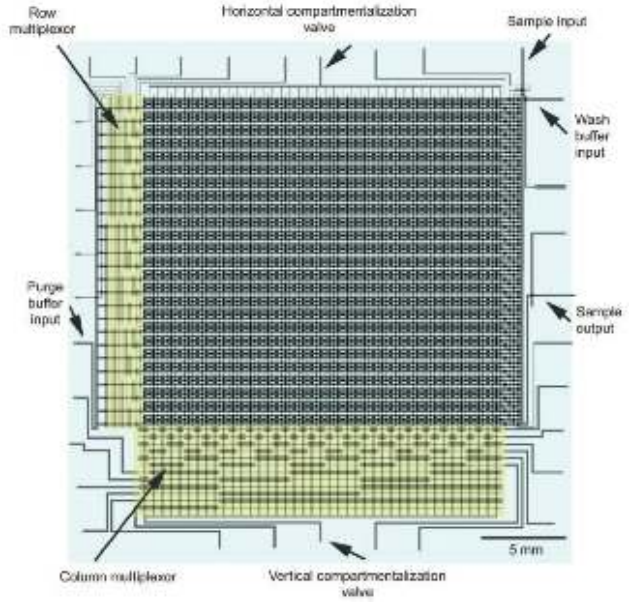

C. Dekker, Nat. Nan. Vol.2, 209 (2007)

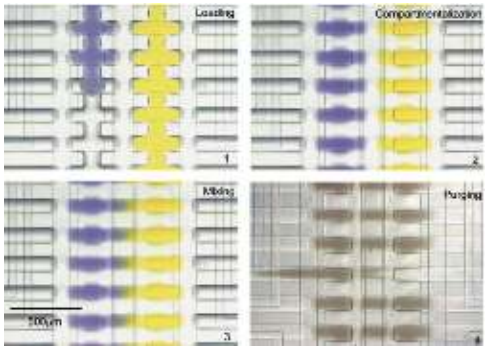
Nanopores

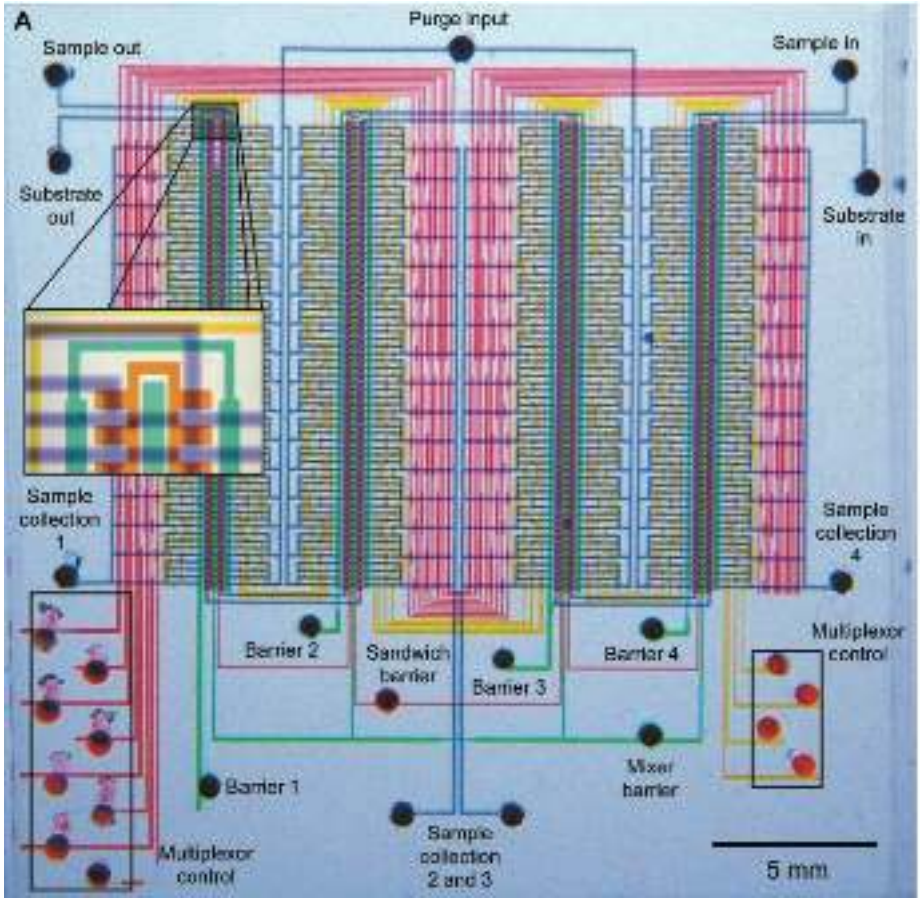
11 September, 2009

FP7 Workshop on Advanced Nanoelectronics

# MicroFluidics on CMOS




S. Quake, Science, Vol.298, 580 (2002)