Workshop on Advanced Nanoelectronics
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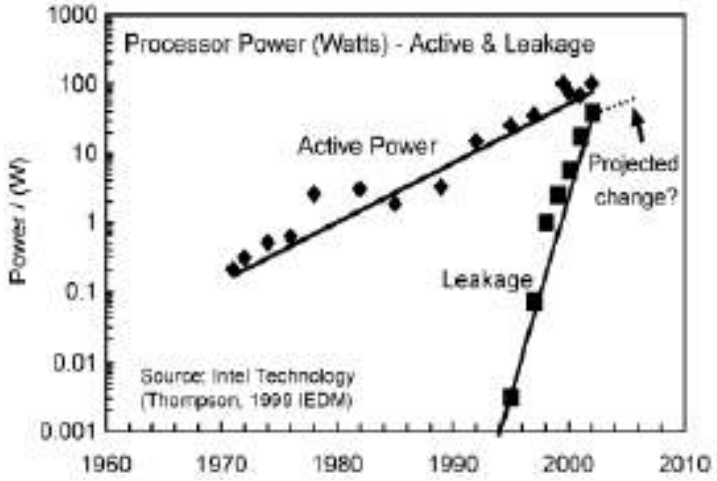
-Sinano Institute vision-

- F. Balestra: *Ultimate CMOS and Memories* (covering part of MM)
- E. Sangiorgi: *Adding functionalities to CMOS* (covering part of MtM)
- O. Engström: *Bottom-up approach, carbon and molecular electronics* (covering part of Beyond-CMOS)

Needs and key challenges

- **Key challenges for future systems:**
  - Scalability/integration
  - Power scaling
  - Heat dissipation
  - Reliability



=> need of green/sustainable highly reliable terascale ICs

⇒ **Links to needs of economy and society:**

-Reduction of electricity supply

-Management of climate warming

-Ubiquitous mobile electronics/communication

-Environment and human monitoring

CMOS landscape

- Need to keep and develop the CMOS expertise in Europe:
  * for technology appropriation
  * to attract more production
  * to enable innovation in electronics systems combining MM and MtM
  * to perform high level trainings and University curricula
  * to prepare the path for future Beyond-CMOS devices which will be integrated together with CMOS on CMOS platforms

- ITRS: minimum size from 25nm in 2007 (65nm technology node) to about 4.5nm in 2022 (11nm node).

- The required performance improvements for the end of the roadmap for high performance, low and ultra low power applications will lead to a substantial enlargement of the number of new materials, technologies and device architectures

- Formidable multidisciplinary challenges for new generations of Nanoelectronic ICs at the most fundamental level (novel materials, new physical phenomena, ultimate technological processes, etc.)

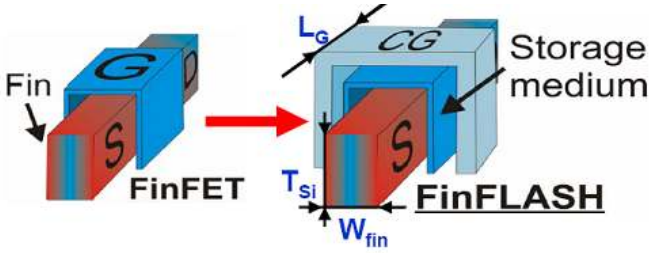
Future EC Workprogrammes

=> Activities applicable to the sub-16nm node range with a high risk factor or a long term industrial perspective, including ultimate More Moore, Non- and Beyond-CMOS and very advanced More than Moore devices integrated on CMOS platforms, to meet requirements of performance, power, functionality and reliability of future electronic systems

Most promising platforms, architectures, technologies, materials

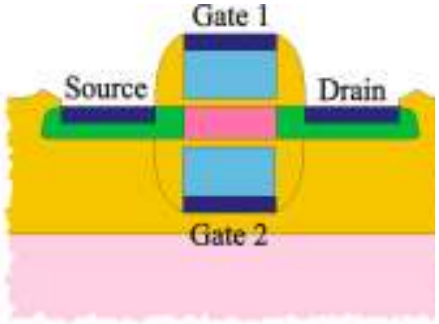
-SOI platforms for thin/ultra thin film fully depleted and multi-gate devices:

increased scalability and performance,
reduced power and variability
(*Europe has pre-eminence in this area*)



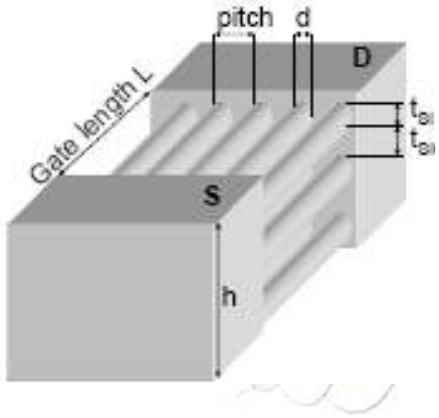
-Multi-gate devices (Double-Gate, Gate-All-Around, FinFETs, etc.):

increased scalability, reduced leakage currents and power consumption, higher performance at constant power, enriched functionality and design flexibility (eg.independent gate operation),reduced impact of intrinsic parameter fluctuations (dopants, LER), increased scaling/performance/reliability of DRAM/SRAM/NVM/Universal Memory, optimised tunnel FETs performance for ultra-low power



-New architectures:

* ***3D integration of Multi-channel MOSFETs/Nanowires***
(Ultimate scaling with control of power and performance, adding functionality and increased sensor sensitivity)
****Novel interconnects*** (RF, optical, CNT)



Most promising platforms, architectures, technologies, materials

-Ultimate lithography:

* EUV (severely delayed and expensive) or
* Imprint lithography

=> *required for feature sizes smaller than 22nm*

-Innovative materials:

* **Channel/substrate materials:** SOI, sSOI, GOI, sGOI, III-V/OI, substrate orientation, high thermal conductivity buried dielectrics
* **Source/drain:** Alternative contacting techniques, e.g. Schottky barriers using new materials
* **Gate stack:** new high k materials/gate stacks for the post 22nm/HfSiO era with chemical stability and low trap density

Challenges in characterization and modelling

- **Issues related to the nanocharacterization of nanoMOSFETs and nanowires:**
  * Physical: roughness, dimensions, strain, dopant imaging, composition and density...
  * Electrical: multiple interfaces and channels, surface states, transport, contacts, single impurity, variability/reliability, new physical mechanisms in very small volumes…

- **Challenges in simulation:**
  * Multi-physics and multi-scale/hierarchical modelling methodologies
  * First principle simulation for band structure
  * Qantum transport
  * Multisubband MC
  * MC calibrated hydrodynamic drift diffusion transports
  *Compact models including quantum and atomic scale effects
  * Account for: holes, thermo electro-mechanical effects, BTB tunnelling, variability
  * Process modelling for new materials and device architectures

Priorities for the European Academe

=> Explore the science and technology aspects for n+4 technology nodes and beyond for understanding new physical phenomena, studying and validating new concepts, novel materials and non-standard processing, innovative device architectures (*using flexible RI*) in order to identify the most promising topics for future information technology and speed up technological innovation

=> Work closely with the *Research Institutes and Industry*

=> This long term research must be supported now in order to prepare the path for future nanoelectronic technologies, as a *15-to-20 years* time frame is usually necessary between the first validation of a new innovative idea and its full demonstration and acceptance into complex systems.

Strategy

=> Europe needs to cover the whole research area underpinning this fundamental technology for the economy of the next decades, recognising that today, *16% of the world economy* is built on electronics products and related services, this percentage is growing every year.