Nanoelectromechanical Switches for Ultra Low Power Applications

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NEMS for Ultra Low Power

- Context
- Nanoswitch state of the art
- Why NEMS are also promising for active power
- Conclusions
NEMS technology is not only promising for leakage power reduction but also for minimizing active power
NEMS for Ultra Low Power

- **Context**
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More Performance… Less Power
Context

Circuit Level Approach

- Parallelism
- Power Gating
- Asynchronous
- Neuromorphic
- Quantum computing
- Adiabatic logic
- Reversible logic

Device Level Approach

- SOI/ FDSOI
- FinFET
- TFET
- III-V FET
- NWFET
- CNTFET
- NEMS
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Nanorelay state of the art

A SYMBOLOGIC ANALYSIS
OF RELAY AND SWITCHING CIRCUITS

by
Claude Elwood Shannon

• The master thesis of Shannon 1937

• The first relay based computer
  Konrad Suze 1941
  2000 relays- 5 Hz
Nanorelay state of the art

- UC Berkeley (T.-J. King Liu, J. Bokor, E. Alon, V. Stojanovic, J. Wu: electrostatic switches)
- MIT (V. Bulovic, J. Lang, T. Swager, organic compressible films)
- Stanford (H.-S. P. Wong, R. Howe: In-plane electrostatic switches, Graphene and CNTs)
- Caltech (M. Roukes, SiC switches)
- Case Western (P. Feng, SiC switches)
- Utah (M. Tabib-Azar, in-plane electrostatic switch)
- UCLA (K. Wang, graphene as structural material)
- UCSD (J. Xiang, NW-NEMFET)
- Rutgers (J. Jeon, Multi-input electrostatic switches and ITO contacts)
- Army Research Labs (L. Currano, PZT piezoelectric switches)
- IBM (D. Newns, P. Solomon, PE/PR switch)
- Intel (K. Kuhn, Electrostatic switches)
- KAIST (J. B. Yoon, electrostatic switches and memories)
- Sogang University (W.-Y. Choi, Memory arrays, FPGA)
- A*STAR (V. Pott, Shuttle ElectroMechanical NVM)
Nanorelay state of the art
Nanorelay state of the art

Source (S) | Gate (G) | Drain (D)

$F_{\text{electrostatic}}$

Contact Resistance

$V_{\text{gate}}$
Contact Resistance Models
Contact Resistance Models

- Asperity Statistics (radius and height, normal or fractal distribution)
- Adhesion forces
- Transport regime (diffusive or ballistic)
Static modeling and optimisation

Berkeley method

\[
E = \left( \frac{\varepsilon A}{g - g_d} + C_i \right) V_{dd}^2
\]

\[
t = \alpha \left( \frac{k}{m} \right) \left( \frac{g_d}{g} \right)^{\gamma} \left( \frac{V_{dd}}{V_{pi}} - \sigma \right)^{-\beta}
\]

\(\alpha\) decreases from 9 to 2 with \(Q\)
\(\beta\) decreases from 1.4 to 0.8 with \(Q\)
\(\gamma\) increases from 0.3 to 0.36 with \(Q\)
\(\sigma \approx 0.8\)

\[
V_{pi} = \sqrt[3]{\frac{8k g_3}{27 \varepsilon A}}
\]

\[
V_{RL} = \sqrt{\frac{2(kg_d - F_A)(g - g_d)^2}{\varepsilon A}}
\]

\(C_i\) interconnect capacitance
\(A\) actuation area
\(FA\) adhesion force

Sensitivity method optimization considering \(E\) and \(t\)

\[
V_{ddopt} = \frac{2\sigma V_{pi}}{2 - \beta}
\]

\(A\) and spring length are also optimized
Nanorelay implementations

Léti

Stanford

Case Western Uni

Berkeley

KAIST
A 500 mV device !!!!

IBM
NEMS Switches

Advantages

• $I_{\text{leakage}} \approx 0$

• Low series resistance
  (problem with scaling)

Disadvantages

• Large Surface area
• Low switching frequency
• High voltage (few volts)
• Reliability issues
• No good Contact resistance models
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Why NEMS are also promising for Active Power Minimization

1. Adiabatic principle is optimal
2. Two solutions: reversible logic or quasi adiabatic logic, but quasi adiabatic logic is generally chosen
3. Quasi adiabatic logic is not interesting with CMOS technology
4. Quasi adiabatic logic is interesting with NEMS technology
Classical Logic (quick reminder)

\[ V_{dd} = iR \]

\[ E_{Dissipated} = \frac{1}{2} CV_{dd}^2 \]
Adiabatic Charging of a Capacitor

\[ E_{\text{adiabatic}} \approx \frac{RC}{T} CV_{dd}^2 \]
Adiabatic Charging of a Capacitor

Conventional Logic

Adiabatic Logic
Adiabatic Charging of a Capacitor

Supply voltage

\[ V_{dd} \]

\[ \text{T} \]

\[ \text{T} \]

\[ A \]

\[ B \]

Output voltage

\[ \text{T} \]

\[ \text{T} \]

\[ \text{T} \]

\[ \text{T} \]

Input A

Input B

Output

\[ \text{T} \]

\[ \text{T} \]

\[ \text{T} \]

\[ \text{T} \]
The Reversible Logic solution

\[ F \xrightarrow{\phi_{l-2}} \frac{G^{-1}}{G} \xrightarrow{\phi_{l+2}} H^{-1} \]

Input \( F \)
Output \( F \)
Output \( G \)
The Quasi Adiabatic solution
Dissipation in Adiabatic CMOS

P. Teichmann, 2012

Inverter circuit in the (a) PFAL and (b) ECRL family

Adiabatic

Non-Adiabatic

Leakage

\[ E_{\text{dissipated}} \approx 2 \frac{RC}{T} CV_{dd}^2 + \frac{1}{2} CV_T^2 + I_{\text{leakage}} V_{dd} T \]
Adiabatic CMOS limitation

**Quasi Adiabatic CMOS**

\[ E_{\text{dissipated}} \approx 2 \frac{RC}{T} CV_{dd}^2 + \frac{1}{2} CV_T^2 + I_{\text{leakage}} V_{dd} T \]

**Conventional CMOS**

\[ E_{\text{dissipated}} \approx \alpha \cdot CV_{dd}^2 + I_{\text{leakage}} V_{dd} T \]

Finally \( \frac{1}{2} CV_T^2 \) and \( \alpha \cdot CV_{dd}^2 \)

Using NEMS it is possible to overcome this limitation
NEMS Based Inverter
NEMS Based Inverter

**Advantages**
- Only 4 NEMS
- Only conventional NEMS
- 4 symmetric phases

**Drawbacks**
- A non adiabatic residual dissipation
- Need having a small $V_{RL}$

\[
E = 2 \frac{R \cdot C_L}{T} C_L \cdot V_{dd}^2 + \frac{1}{2} C_L \cdot V_{RL}^2
\]
Comparison with CMOS

\[ E = 2 \frac{R_{nems} \cdot C_L}{T} C_L \cdot V_{dd}^2 + \frac{1}{2} C_L \cdot V_{RL}^2 \]

\[ E \equiv 2 \frac{R_{cmos} C_L}{T} C_L V_{dd}^2 + \frac{1}{2} C_L V_T^2 + I_{leakage} V_{dd} T \]
Comparison CMOS-NEMS

To evaluate the normalized dissipated energy for different CMOS and NEMS technologies, the graph plots frequency (MHz) on the x-axis and normalized dissipated energy on the y-axis. The x-axis ranges from $10^{-1}$ to $10^{3}$ MHz, while the y-axis ranges from $10^{-3}$ to $10^{2}$. The graph compares Conventional CMOS, Adiabatic CMOS, Adiabatic high resistance NEMS, and Adiabatic low resistance NEMS, with activity factors indicated for Conventional CMOS as 0.1 and 1.
NEMS technology is not only promising for leakage power reduction but also for minimizing active power.

However it is necessary to have a reliable scaled relay technology…….
Thank You.
Questions ?