III-V-MOS

News from the European *Technology CAD for III-V Semiconductor-based MOSFETs* Research team at month 25

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III-V-MOS is an EC funded project aiming to provide the European Semiconductor Industry with accurate device simulation methods and models, integrated into TCAD tools, for successful introduction of optimized device designs based on III-V n-MOSFETs in CMOS technology at and beyond the ITRS 14nm node.

WP1 Management, Dissemination and Exploitation
leader: L. Selmi, IUNET

WP2 Physics based models and verification
leader: A. Schenk, ETHZ

WP3 Characterization
leader: L. Czornomaz, IBM

WP4 TCAD models and verification
leader: F. Bufler, Synopsys

WP5 Device level performance investigation
leader: D. Esseni, IUNET

WP6 Application by end users
leader: T. Herrmann, GLOBALFOUNDRIES

Objective 1 > "High level" models to explore III-V n-MOSFETs beyond the 14nm technology node

QuantumWise: band structure of random III-V alloys

In a perfectly periodic crystal Bloch's theorem applies, and the wave number **k** is a good quantum number. Each band is a line with zero width in both the E- and **k**-directions. In a disordered alloy (e.g., $In_xGa_{1-x}As$) one cannot *a-priori* know if **k** is still a good quantum number or if the whole concept of a band structure is well defined. In III-V-MOS, QuantumWise has investigated this aspect by calculating "effective band structures" (EBS, [1,2]) with its atomistic DFT simulator ATK.

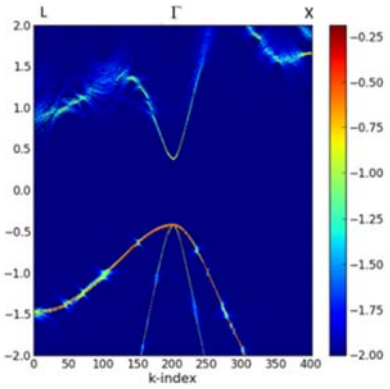


Figure 1 : InGaAs EBS showing the effect of random alloy.

A large super cell made of a 4x4x4 repetition of the primitive FCC unit cell (128 atoms) is considered where some of the Ga atoms are replaced at random with In atoms while always keeping the In/Ga ratio fixed at 0.53/0.47. From the band structure of the super cell containing more than 1000 bands one can "unfold" the band structure to only contain the bands corresponding to the primitive cell. Sample averaging over different realizations of the random configurations in the super cell yield an average band structure *density*, representing the EBS. As shown in a logarithmic colour scale in Figure 1, the conduction band is well defined around the Γ-point, where the band is narrow, while it is much less well-defined at the L- and X-point valleys. A band broadening as large as 60 meV was estimated for the L- and X-point valleys. The result can be understood in terms of the long wavelength states present at the Γ-point. The local random variations "are not seen" by a long wavelength electron. Contrary, at the X- and L-points, the wave functions vary on the atomic scale and the disorder affects the energy and wave function.

[1] V.Popescu et al., *Phys. Rev. Lett.,* vol. 104, p. 236403, 2010, and *Phys. Rev. B,* vol. 85, p. 085201, 2012.
[2] M.W.Haverkort, I.S.Elfimov and G.A.Sawatzky, *arXiv:1109.4036,* 2011.

ETH-Zurich: Investigation of leakage current mechanisms

Due to the small effective mass compared to silicon, tunneling phenomena can cause prominent leakage currents in III-V MOSFETs. ETHZ has performed an extensive study of the source-to-drain tunnelling (SDT) and band-to-band tunnelling (BTBT) leakage in FinFET and nanowire structures. For this, the OMEN full-band and atomistic quantum transport solver [3] has been used. Starting from the specifications given by the ITRS for the year ~2020 the geometrical and structural parameters of double-gate InGaAs ultra-thin-body FETs have been changed to understand their influence and to give recommendations for the transistor design. The results suggest that BTBT will become an issue only in transistors with ultra-short channel lengths (below 10 nm) and/or with a thick body. The most severe effect originating from the small transport effective mass is SDT (Figure

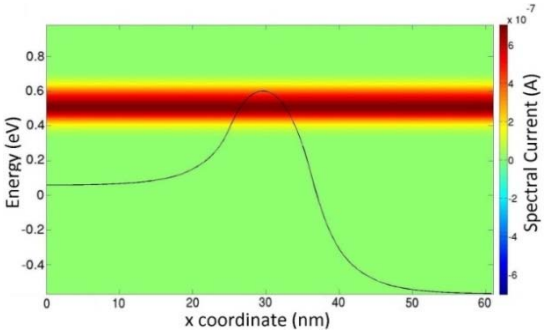


Figure 2: Spectral current in a double gate ultra-thin body (DG-UTB) FET with L_G = 10nm showing strong source-to-drain tunneling (SDT).

2) which deteriorates the sub-threshold characteristics when the gate length is scaled down. It is therefore a goal of utmost importance to design devices that are as little sensitive as possible to this undesired effect. To this end, the band gap of the channel material should be slightly larger than the applied drain bias V_{DS} in order to minimize BTBT. With $In_{0.75}Ga_{0.25}As$ and V_{DS}=0.68 V, this requirement is not satisfied. Selecting an Indium concentration lower than 50% is not suitable either since the advantage of III-V over Si, a small transport effective mass, diminishes. ETHZ simulations have shown that $In_{0.53}Ga_{0.47}As$ represents a good compromise between improved transport properties and low leakage currents. As regards the gate design: whereas the overlap of source and drain doping regions with the gate contact has been widely used by the semiconductor industry in the past to boost the transistor ON-current, in ultra-short devices it has a negative impact on the sub-threshold slope by effectively reducing the width of the potential barrier separating the source and drain extensions and thus enhancing the SDT probability. The opposite approach called "gate underlap" where the doped source and drain regions are separated from the gate contacts by a ~ 1-2 nm offset, widens the potential barrier, and consequently reduces the sub-threshold swing (SS). ETHZ results (Figure 3) clearly show that a SS of 70-75 mV/dec will either require longer gate contacts, a strong gate underlap, a better electrostatics control through a triple-gate or gate-all-around configuration, or a combination of all these approaches.

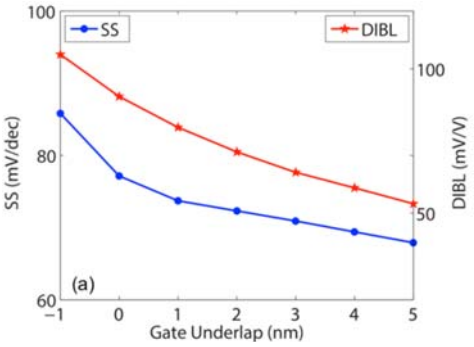


Figure 3: SS and DIBL in a DG UTB FET with L_G = 15nm as a function of the length of the gate underlap region L_{und}. L_{und} <0 indicates gate overlap instead of underlap.

[3] M. Luisier, Phys. Rev. B 74, 205323, 2006.

Objective 2 > Breakthrough integration schemes for InGaAs on Silicon

IBM: InGaAs on Si technology platform for CMOS

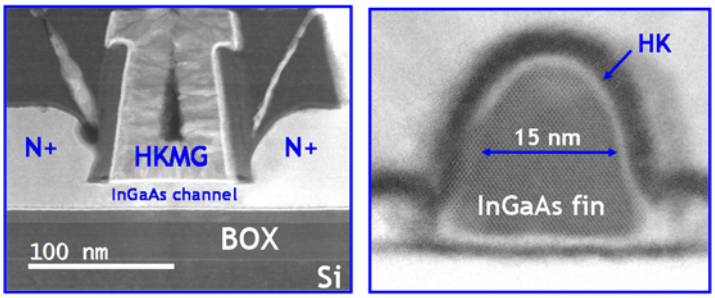


Figure 4: InGaAs UTB SOI and Fin MOSFETs

At the VLSI Technology Symposium in June 2015, IBM reported latest developments on its InGaAs on Si technology platform [4,5].

Firstly, IBM demonstrated the template assisted selective epitaxy of InP and InGaAs in empty SiO_2 cavities on Si. This technique enables the fabrication of micron-sized islands of InGaAs on standard 300 mm bulk or SOI wafers. The obtained InGaAs-on-insulator films can be processed into CMOS-compatible gate-first FinFETs ([4] and Figure 4). Secondly, IBM reported a method to realize high-quality 200 mm InGaAs-on-insulator wafers by means of direct wafer bonding. A thick strain-relaxed buffer is used to integrate the InGaAs channel on a large Si donor wafer, which is bonded and transferred on a target 200 mm Si wafer with a thin buried oxide. The obtained crystalline quality is among the best reported ones for InGaAs on large-scale Si.

Finally, two leading industrial integration schemes were evaluated on CMOS-compatible self-aligned InGaAs FinFETs: gate-first (GF) and replacement-metal-gate (RMG). In the GF scheme, the high-k/channel interface is subjected to the high thermal budget of the source/drain formation which degrades the interface quality. In the RMG scheme, a dummy gate is used during the high temperature formation of source/drain regions, which is later removed and replaced by the final high-k and metal gate layers. As such, the high-k/channel interface is not exposed to high temperatures, which translates in largely improved interface quality. As a result, InGaAs FinFETs on Si with a RMG, 50 nm gate lengths and 15 nm fin width demonstrate record on-state and subthreshold performance among all CMOS-compatible self-aligned InGaAs MOSFETs on Si. Those advanced InGaAs FinFETs can be integrated on top of high-performance SiGe-OI FinFETs in a 3D Monolithic integration scheme. Those results will be reported at the forthcoming IEDM 2015, in the III-V-MOS paper 8.8.

[4] L.Czornomaz et al., Proc. VLSI Technology Symposium, 2015, pp.13.3.
[5] V.Djara et al., Proc. VLSI Technology Symposium, 2015, pp.13.3.

IMEC: First FinFETs on Si in a 300mm pilot-line

First InGaAs FinFETs have been demonstrated on 300mm Si substrates and using process modules, compatible for future CMOS high-volume manufacturing [6]. The integration flow is based on the fin replacement process, which allows possible co-integration of these high mobility materials with Si and (Si)Ge channels. First devices showed a SS of 190 mV/dec and extrinsic transconductance g_m=558 µS/µm

(*V*ds=0.5 V) for an EOT of 1.9nm, a L_G=50nm and a measured fin width of 55nm. A trade-off between off-state leakage and mobility for different p-type doping levels of the InP and InGaAs layers was found while the Replacement Metal Gate (RMG) high-κ last processing was demonstrated to offer significant performance improvements over that of high-κ first. With small modifications to the process flow, InGaAs gate-all-around (GAA) devices were also demonstrated [7]. An extrinsic g_m=1030 $\mu S/\mu m$ at *V*ds=0.5 V was achieved, which is an almost 2× increase compared to the FinFET devices. This improvement was attributed to the elimination of the Mg p-type doping in the GAA flow. Ultra-scaled nanowires with diameters down to 6 nm, fabricated using the same process, showed immunity to D_{it} resulting in an SS of 66 mV/decade and negligible drain-induced barrier lowering for devices with gate lengths of 85nm.

[6] N. Waldron et al., "An InGaAs/InP Quantum Well FinFet Using the Replacement Fin Process Integrated in an RMG Flow on 300mm Si Substrates", VLSI Symp. 2014.
[7] N.Waldron et al., « InGaAs GAA nanowire devices on 300mm substrates«, IEEE EDL, pp.1097, 2014.

Objective 3 > Development of TCAD models for the simulation of III-V materials.

IUNET: Mobility model for UTB InGaAs on InP MOSFETs

IUNET has recently developed a simple, analytical electron mobility model at low longitudinal fields to be integrated in TCAD tools. The model addresses ultra-thin-body (UTB) MOSFETs integrating an $In_{0.53}Ga_{0.47}As$-on-InP semiconductor channel with 5-15 nm $In_{0.53}Ga_{0.47}As$ thickness (T_B), and Al_2O_3 gate oxide. In order to validate the model, devices fabricated and characterized at IMEC are considered.

For a reliable estimation of mobility vs. inversion charge, a careful assessment of interface trap density is necessary. This can be done once the concentration of fixed and trapped interface charges, not negligible in III-V MOSFETs, is determined through comparison of simulated and experimental C_G-V_{GS} data (Figure 5). To this aim, a T_B-dependent amount of interface traps are introduced, representing the so-called acceptor border traps in the conduction band. The TCAD data accounts for density-gradient (DG) quantum corrections. The DG model was preliminary calibrated on the Schrödinger-Poisson solution.

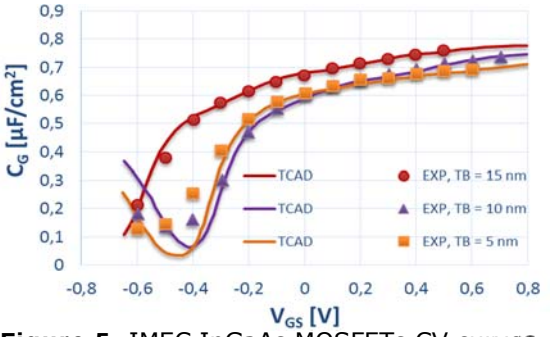


Figure 5: IMEC InGaAs MOSFETs CV curves

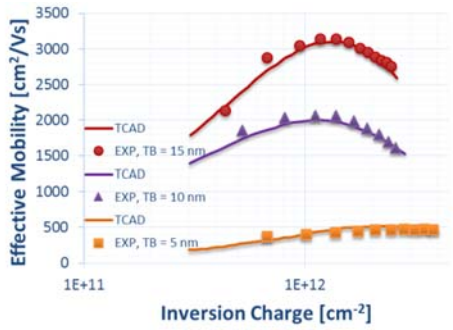


Figure 6: Mobility model vs. experiments.

The mobility model is empirical but physically based and accounts for the main scattering sources occurring in such devices, namely Coulomb centers, phonons and surface roughness. The thin-body effective thickness, which impacts the phonon scattering and is modulated by the transverse (vertical) electric field at varying V_{GS} through quantum effects, is also taken into account. The model has been calibrated on the experimental data extracted from the $In_{0.53}Ga_{0.47}As$ MOSFETs characterized at IMEC (Figure 6). The calibrated mobility model, integrated in the Synopsys Sentaurus Sdevice TCAD simulator through the Physical-Model Interface has been used to compare device simulations with I_{DS}-V_{GS} experimental data [8].

[8] G. Betti Beneventi, et al., IEEE Trans. on Electron Devices, Vol. 52, Issue 11, pp. 3645 – 3652, 2015.

Synopsys compares InGaAs to Si by Monte Carlo FinFET simulation

For a realistic performance comparison between silicon and $In_{0.53}Ga_{0.47}As$ FinFETs TCAD device simulations need to consider all relevant physical effects and realistic geometry and doping profiles such as, for instance, the ones for SOI FinFETs illustrated in Figure 7 and suggested by the III-V-MOS technological partner IBM. For the simulation of InGaAs-FinFETs, the Monte Carlo approach is the method of choice since it includes the quasi-ballistic transport of small-mass materials in short-channel devices on a physical basis.

In this study, the III-V-MOS partner Synopsys has used a full-band structure computed with the nonlocal empirical pseudopotential method. Scattering comprises elastic acoustic intravalley and inelastic intervalley phonon scattering, anisotropic polar-optical phonon scattering, ionized impurity scattering and surface roughness scattering. The quantum correction is based on 2D Schrödinger-Poisson solutions on the cross-section of the fin. Fermi-Dirac statistics is important for InGaAs due to the small effective density-of-states (N_C) and is treated according to the scheme in [9].

In contrast to Maxwell-Boltzmann statistics, Fermi-Dirac statistics leads to a decrease of the low-field mobility for increasing electron density also in the absence of impurity scattering [10]. However, we found that computing the Fermi energy for a given density according to the relation $n=N_C F_{1/2}(\eta)$, which is derived under the assumption of a parabolic band, strongly underestimates the mobility. Therefore it is necessary to numerically evaluate the Fermi energy using explicitly the full-band density-of-states, a new feature which is enabled in the upcoming Synopsys TCAD release L-2016.03.

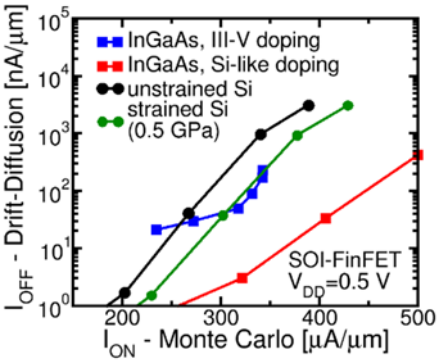


Figure 8: I_{OFF}-I_{ON} relation for Si and InGaAs n-FinFETs.

Full-band Monte Carlo simulation is then used to compare (strained) Si and unstrained InGaAs FinFETs. In the case of InGaAs two doping configurations are considered. On the one hand, the typical III-V configuration shown in Figure 7 and on the other hand a Si-like doping where only the maximum S/D doping in Si of $2x10^{20}$ cm^{-3} is reduced down to $3x10^{19}$ cm^{-3} in order to study the material-effect separately. The corresponding I_{OFF}-I_{ON} relations are shown in Figure 8. It can be seen that InGaAs with a similar doping profile as in silicon features a strong performance improvement. However, in case of typical III-V doping profiles, InGaAs device performance is reduced and similar to that of strained silicon devices, since the absence of extension doping under the spacer involves a high resistance. This shows that geometry and doping profile optimization are especially relevant to achieve superior InGaAs device performance.

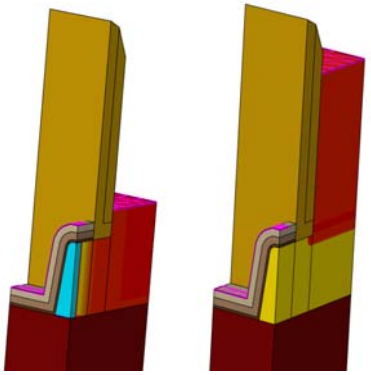


Figure 7: Realistic Silicon (left) and InGaAs (right) n-FinFETs used in TCAD simulations. L_G = 15nm, H_{Fin} = 20nm, W_{Top} = 5.5, taper angle=7°. The InGaAs device has the same basic geometry as the Silicon one, but raised S/D and lowly doped n-type (instead of p-type) channel.

[9] E.Ungersboeck and H.Kosina, Proc. SISPAD, Tokyo (Japan), Sept. 2005, p. 311.
[10] F.M. Bufler, SINANO Workshop on "New Materials for Nanoelectronics" at ESSDERC 2015, Graz (Austria), http://www.iii-v-mos-project.eu/dissemination/workshops-conferences/iii-v-mos-presentations-at-the-sinano-workshop.html

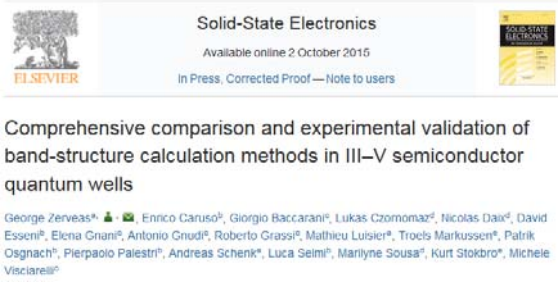
Objective 4 > Transfer of technologies and knowledge

QuantumWise: New software release and hands-on demo

QuantumWise, project partner responsible of atomistic density functional theory (DFT) calculations, has in October 2015 released a new version of its softwares, Virtual NanoLab and ATK, with special focus on the atomic-scale modelling of III-V semiconductor devices and materials. The release includes modules exploiting the know-how developed in the III-V- MOS project. Virtual NanoLab is now available free of charge to academic users; a "hands-on" dissemination session was held at the ESSDERC 2015 Workshop on "New materials for nanoelectronics" in Graz to present it.

Among the several new features are the Virtual Crystal Approximation (VCA) for DFT and the Effective band structure (EBS) analysis (zone unfolding) for supercells of e.g. random alloy $In_xGa_{1-x}As$ described above. VCA and EBS offer complementary simulation possibilities particularly useful for modelling $In_xGa_{1-x}As$. The VCA makes it easy to calculate the energy bands for any alloy composition, provided that the band structure is well-defined (i.e., neglecting randomness). The EBS calculations on the other hand includes the randomness of In and Ga. Additional new features relevant for the III-V MOS project includes electron-phonon interaction for device simulations as well as bulk mobility calculations.

Joint Open Access publication by project partners


Solid-State Electronics
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In Press, Corrected Proof — Note to users

Comprehensive comparison and experimental validation of band-structure calculation methods in III–V semiconductor quantum wells

George Zerveas, Enrico Caruso, Giorgio Baccarani, Lukas Czornomaz, Nicolas Daix, David Esseni, Elena Gnani, Antonio Gnudi, Roberto Grassi, Mathieu Luisier, Troels Markussen, Patrik Osgnach, Pierpaolo Palestri, Andreas Schenk, Luca Selmi, Marilyne Sousa, Kurt Stokbro, Michele Visciarelli

A comprehensive study of band structure calculation methods for bulk and ultra thin $In_xGa_{1-x}As$ films and comparison with experimental ellipsometry bandgap data has been recently published by the consortium partners on Solid State Electronics DOI: 10.1016/j.sse.2015.09.005 . Consistently with the open strategic approach implemented by the project the publication is Open Access.

This project has received funding from the European Union's Seventh Framework Programme under grant agreement n° 619326.