Press release

New Computer Aided Design solutions to reduce cost and time to market of high performance energy efficient nanoelectronic technology

Udine/Italy, December 2013,

Enabling fast and effective design of new transistors for high performance electronics with greatly reduced power consumption. This is the ambitious objective that a unique multidisciplinary team of scientists and engineers from five European countries and eight Research institutions, Universities and industrial R&D labs will pursue in the next three years under the leadership of the Italian university consortium for nanoelectronics, IUNET, in the framework of the EC funded project **III-V-MOS *"Technology CAD for III-V Semiconductor-based MOSFETs"***.

Nanoelectronics is recognized as a key enabling technology with profound impact on all aspects of our daily life, in particular in the fields of communication, computing, consumer electronics, health, transport, environment and secure societies. To sustain the progress of high-performance energy-efficient nanoelectronics, a new scenario is currently pursued by the industry worldwide where innovative devices based on so called III-V compound semiconductor materials will replace in part conventional silicon transistors. The integration of III-V devices into silicon platforms may reach production as early as 2018 but, for this scenario to become reality, accurate technology computer aided design (TCAD) tools will be necessary. In fact nanoelectronics relies on intensive use of TCAD to cut development costs and significantly reduce time to market.

The III-V-MOS project consortium addresses this need for advanced TCAD and will provide the European Semiconductor Industry and the European nanoelectronics research centers with dependable, accurate and calibrated models and methods, integrated into user friendly simulation tools, for timely and successful introduction of the new III-V devices in mainstream nanoelectronics technology.

The project builds upon the strong modeling and simulation expertise of European academic partner institutions (IUNET consortium and ETH-Zurich). Future exploitation and high impact of the project results are guaranteed by the TCAD market leader (Synopsys); by a SME specialized in the growing business of atomistic simulations for technology development (QuantumWise - Denmark); by a research center (IMEC - Belgium) and an industry lab (IBM Research - Zurich) and by the European silicon foundry GLOBALFOUNDRIES Dresden. The SINANO Institute will set up effective strategies for dissemination of project results and completes the partners list.

The FP7 Programme
FP7 is the short name for the Seventh Framework Programme for Research and Technological Development. This is the EU's main instrument for funding research in Europe beginning in 2007. The III-V-MOS is a Collaborative Project selected during the last Call of FP7.

The III-V-MOS consortium partners:

Academic institutions:
- Consorzio Nazionale Interuniversitario per la Nanoelettronica IUNET (Italy – project coordinator)
- Eidgenoessische Technische Hochschule, ETH Zurich (Switzerland),

Research Center:
- Interuniversitair Micro-Electronica Centrum VZW (Belgium)

Research Institute
- SiNANO Institute (France)

Industrial Organization
- IBM Research GmbH (Switzerland)
- QuantumWise A/S (Denmark)
- GLOBALFOUNDRIES Dresden Module One LLC & Co. KG (Germany)
- Synopsys Switzerland LLC (Switzerland)

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For full project documentation please visit: http://www.iii-v-mos-project.eu