University of Liverpool

Multilevel Cell (MLC) Switching in RRAM Devices

Multilevel cell (MLC) is a memory cell that can store more than a single bit of data as in a conventional memory cells. The devices can store 2 or more bits of data in a single cell, resulting in an increase in data storage density and reducing the cost per unit of storage. 3-bit and 4-bit MLC flash memory cells have been commercialized in past few years by Samsung, SanDisk, and Line-On using the NAND flash memory technology. However, RRAM MLC, still in ongoing research, can increase the data density further due to one-transistor one-resistor (1T1R) configuration and can further reduce the cost per unit of storage due to ease of fabrication compared to standard NAND technology. In University of Liverpool, a 3-bit MLC switching RRAM has been developed based on atomic layer deposited (APL) Ta_2O_5 doped with nitrogen. The state-of-the-art device shows 8 well separated intermediate switching states (3 bits) with variability less than 30 %.

The MLC in RRAM can be performed by two methods. The more common method is by changing the set current compliance which creates intermediate low resistance states (LRS) in upper region of memory window (Fig. 1). The other, less explored, method is by changing the maximum voltage during reset which generates intermediate high resistance states (HRS) in lower region of memory window (Fig. 2). There are two requirements for MLC in memory cells in general and in RRAM cells in particular: a wide memory window to accommodate larger number of intermediate states, with enough separation or margin between the states, and high state stability to prevent intermixing of the states. Liverpool group has shown that doping the oxide layer in RRAM MIM structure with nitrogen or fluorine increases both the memory window and the states stability significantly which enables these devices for MLC applications. An approach of combining two methods of MLC in RRAMS (set current compliance and maximum voltage during reset) has been used by Liverpool team to achieve 8 well separated states (3-bit) with variability of less than 30 % in nitrogen doped Ta_2O_5 RRAM devices (Fig. 3).

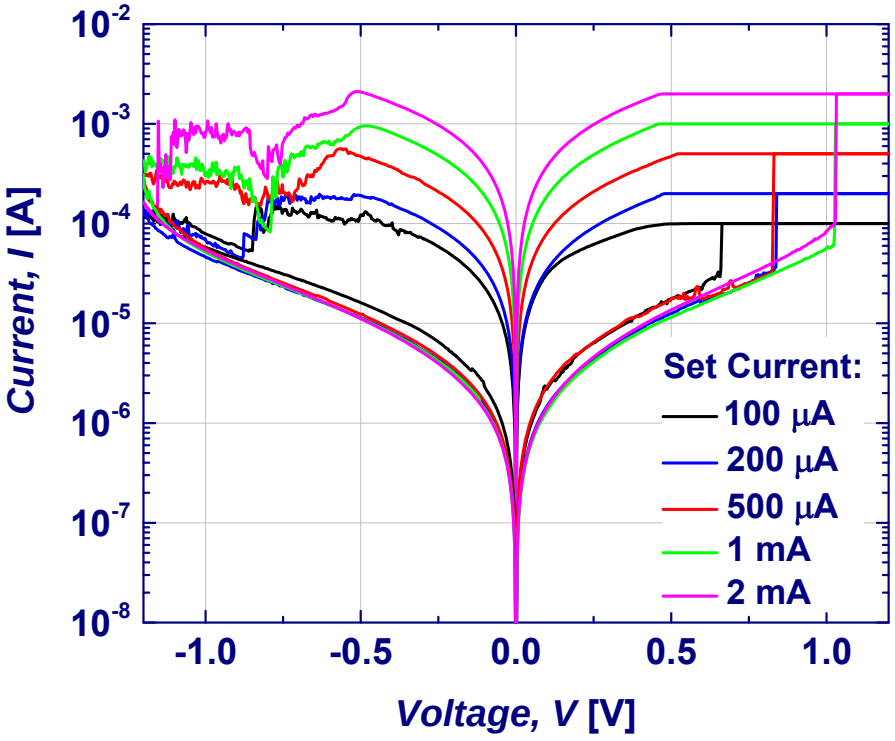
Current, I [A]
Voltage, V [V]
Set Current:
100 µA
200 µA
500 µA
1 mA
2 mA

Fig. 1

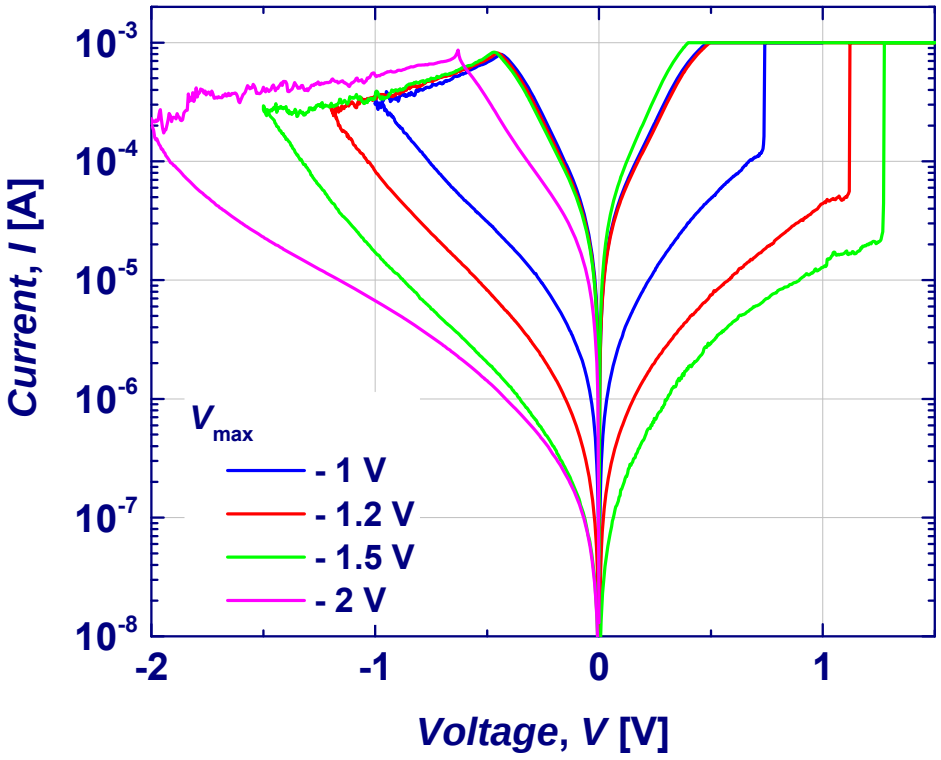
Current, I [A]
Voltage, V [V]
V max
- 1 V
- 1.2 V
- 1.5 V
- 2 V

Fig. 2

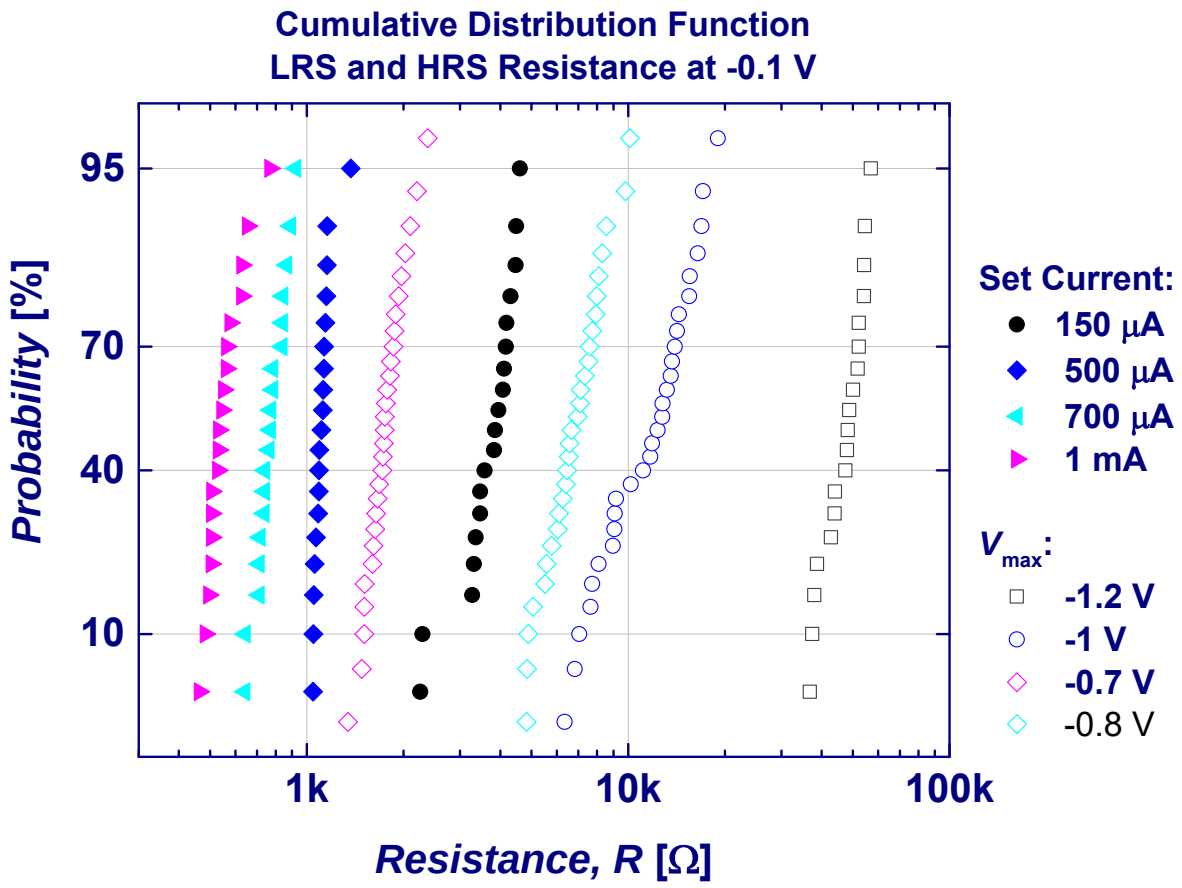
Cumulative Distribution Function
LRS and HRS Resistance at -0.1 V
Probability [%]
95
70
40
10
1k
10k
100k
Resistance, R [Ω]
Set Current:
150 µA
500 µA
700 µA
1 mA
V max:
-1.2 V
-1 V
-0.7 V
-0.8 V

Fig. 3