III-V-MOS

Technology CAD for III-V Semiconductor-based MOSFETs

This project has received funding from the European Union's Seventh Framework Programme under grant agreement n° 619326.

The project: aims to provide the European Semiconductor Industry with accurate device simulation methods and models, calibrated to high quality hardware and integrated into TCAD tools, for timely and successful introduction of III-V compound semiconductor n-MOSFETs in CMOS technology.

Context: III-V compound semiconductor n-type MOSFETs are expected to enter production in 2018. Accurate simulation models and methods constitute a prerequisite to benefit from the advantages that Technology CAD can bring in the early stages of industrial development. The III-V-MOS project targets this demand of dependable TCAD, and delivers to the European Semiconductor Industry new device simulation methodologies enabling the use of quantum drift-diffusion and Monte Carlo TCAD tools calibrated on the best available hardware.

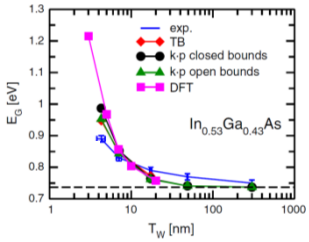
Objectives

WP2

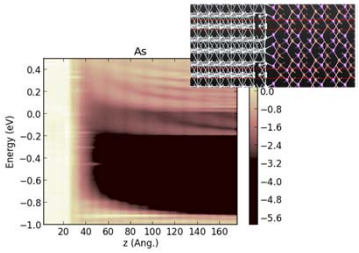
- **To develop comprehensive "high-level" tools for III-V n-MOSFETs and a material parameter database forming the ground for TCAD compact model development.**

Results

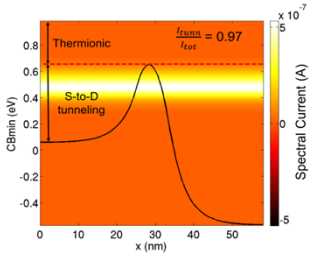
Band structure database *for accurate simulation of* ***relaxed and strained $In_xGa_{(1-x)}As$ alloys.***



Understanding *$In_xGa_{(1-x)}As$ and InAs thin films, Metal/InGaAs contacts and Al2O3/InGaAs interfaces* ***by atomistic DFT and TB simulation.***



Semi-classical and full-quantum «high-level» device ***simulators reveal the physical mechanisms limiting III-V MOS device scaling.***

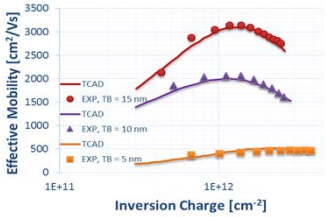


WP4

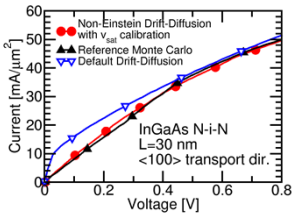
- **To develop, validate and calibrate TCAD compact models for III-V semiconductor n-MOSFETs forming the base for accurate and predictive quantum drift diffusion and Monte Carlo TCAD simulations.**

Results

TCAD Compact model for Quantum Drift Diffusion (QDD) mobility simulation *of thin $In_xGa_{(1-x)}As$ films on InP* ***developed and calibrated.***



TCAD QDD with non-Einstein diffusivity *yields accurate drain current of short devices at low V_{DS}.*

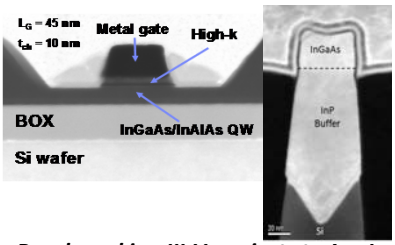


WP3,5

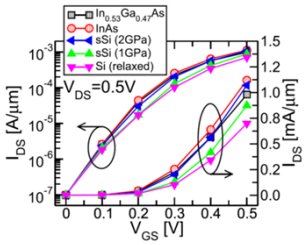
- **To narrow down the technology options for III-V n-MOSFETs by exploring the viable optimization scenarios and by identifying the most promising device designs.**

Results

High performance ***$In_{0.53}Ga_{0.47}As$ FDSOI, FinFET and Nanowire test structures and MOSFETs integrated on 200/300mm Silicon wafers.***



Benchmarking III-V against strained Silicon MOSFETs at L_G=14nm



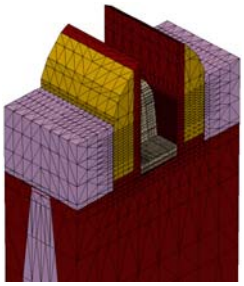
WP6

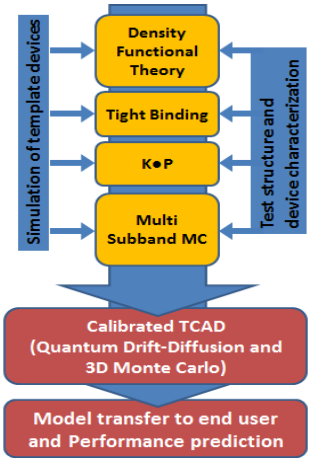
- **To deliver to end users in semiconductor manufacturing industry and nanoelectronics research labs quantum drift diffusion and Monte Carlo TCAD setups for comparison with available hardware.**

Results

Atomistic DFT models transferred *into official Quantumwise ATK product releases.*

3D Monte Carlo simulation setups for realistic FDSOI and FinFETs transferred *into official Synopsys Sentaurus product releases.*





The III-V-MOS project integrated modeling approach

Looking ahead – What's next ?

Model calibration and verification

Strained III-V device design options

Performance benchmarking

Transfer of models, simulation setups and technology to industrial partners

Contacts:

Project coordinator: Luca Selmi, University of Udine, Italy **Email:** luca.selmi@uniud.it

Project office: Pascale Caulier, SINANO Institute, Grenoble, France **Email:** Pascale.Caulier@minatec.grenoble-inp.fr

www.iii-v-mos-project.eu