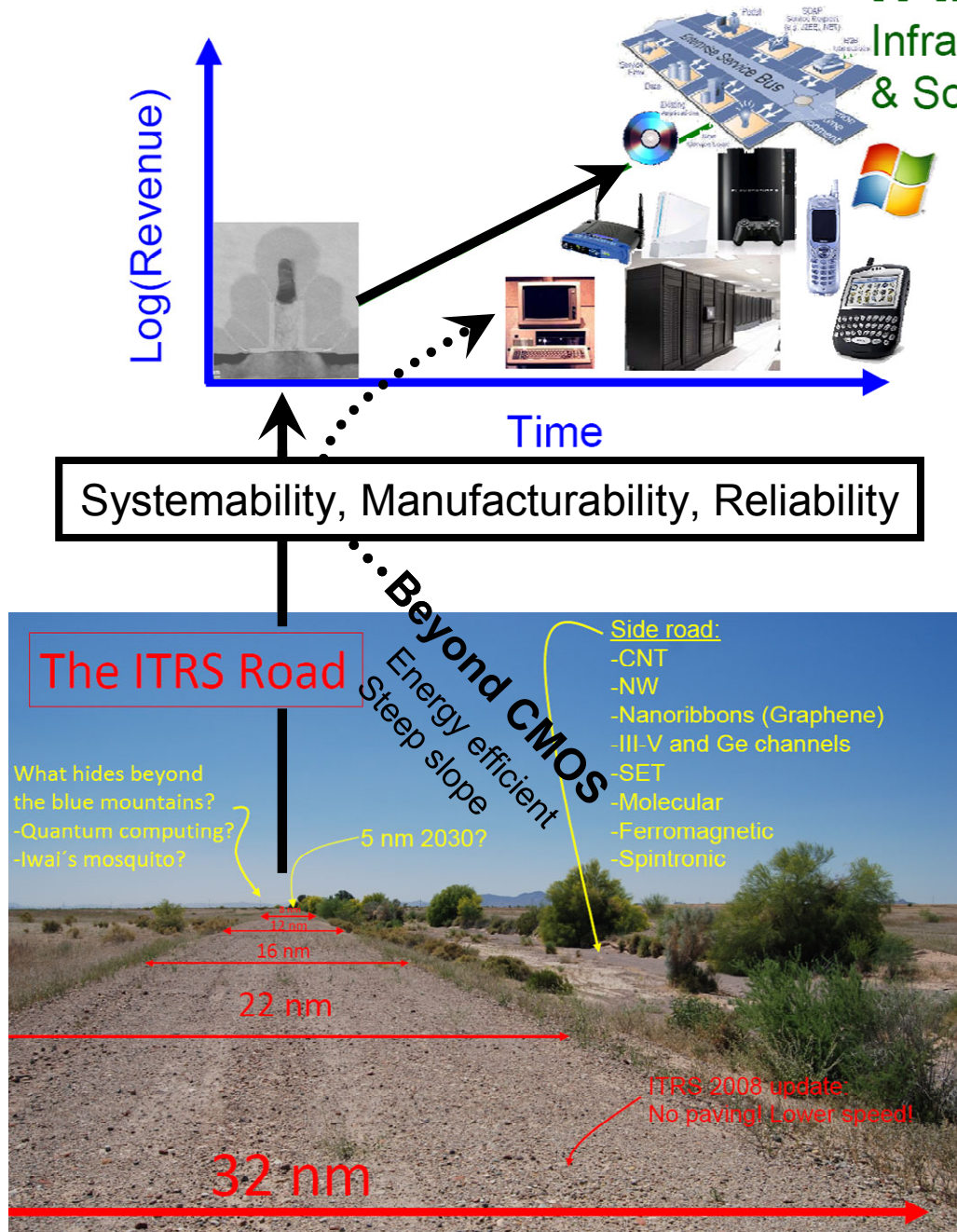


FP7 Workshop on Advanced Nanoelectronics Technologies

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IT Industry:
Infrastructure
& Solutions



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1. Introduction

Computing and communication technologies, supported by strong progress in nanoelectronics, have proven as pervasive, driving forces in the world economy over the past two decades. They affect nearly every aspect of life: education, entertainment, transportation, workplace and personal communication to the basic infrastructures of our economy and society at large. Today 16% of the world economy is built on electronic products and related services and this percentage is continuously growing. Society has come to depend not just on basic functionalities of computing and communication but on their significantly increased capabilities that have been made available each year at given cost and power budget.

Today the applications covered by advanced silicon CMOS technology are enabled by the aggressive scaling of the MOS transistor (MOSFET) and the reduction of the cost per transistor by the amazing factor of 10^6 in more than 40 years, a level never reached by any other modern technology. ITRS played a major role in defining the specifications to be reached by the silicon MOSFET in order to fulfil criteria for mobile computing and mobile communications (e.g. high performance - HP, low power - LP, low standby power - LSTP), see Fig. 1. However, serious and simultaneous barriers are expected to significantly slow-down the evolution of CMOS by 2020: fundamental limits of devices and materials, system level limits, power density issues and cost. Thus, discussing and identifying a more visionary thinking about future applications and their potential technology/device/circuit/system enablers (see Fig. 1) in order to accordingly shape future calls of the European Commission's research programme in nanoelectronics, is very timely.

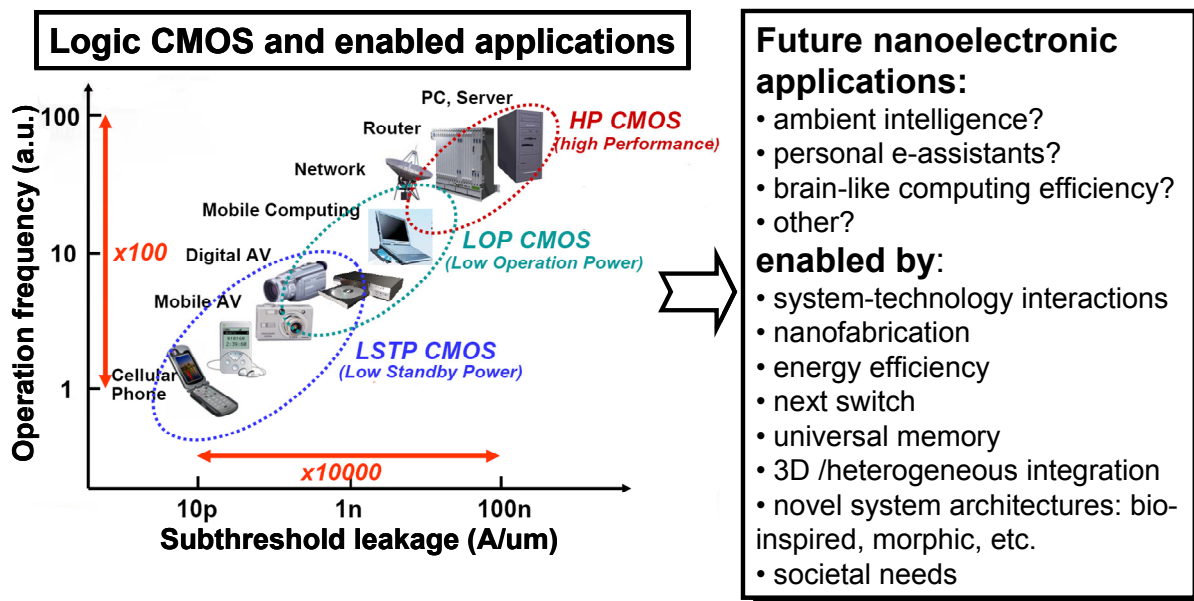


Figure 1: Left: Present applications enabled by the advanced silicon CMOS its main figures of merit (operation frequency and sub-threshold leakage). Right: expectations for future nanoelectronics applications and their enablers. One aim of the workshop was to foster such novel system-technology interactions and thinking as enabler of a long term vision for nanoelectronics.

The main idea was to discuss in a workshop the system-technology interaction as one of the main drivers for innovation in nanoelectronics and receive academic and industrial feedback concerning world wide and European trends and priorities in nanoelectronics. Moreover, the future development of true ambient intelligence systems everywhere, with nanoelectronics penetrating all aspects of everyday life, from the individual to the society, will create novel challenges for the system architectures and supporting technologies.

The reasons for organizing the workshop have been well pre-defined and explained by DG INFSO/Nanoelectronics and can be summarized as follows:

- Input to a WP 2011-2013 which will also lead us to the new FP8 and is not just a continuation or ending of FP7;
- Come to stronger support of the academic community in the area of nanoelectronics;
- Enlarge the academic community dealing with advanced nanoelectronics devices and processes with the academic community dealing with advanced circuits and systems;
- Enhance cooperation between the different elements of the food chain from materials and devices through to circuits and architectures, design, integration of novel devices and to advanced (sub-)systems.
- Foster system-level thinking and long term multi-disciplinary research by the academic community guided by or agreed with the industry.

The concrete goals of the workshop have been:

- To identify the major technical and scientific challenges and drivers of future nanoelectronics in the More Moore, Beyond CMOS and More Than Moore domains based on feedback coming from the academic and industry communities;
- To discuss approaches and choices to position and embed the FP7, and potentially FP8 ICT calls, in a landscape of programmes as Eureka/Catrene, Eniac, Artemis, FP7 NMP as well as national and regional programmes
- To describe the change in the R&D business models in the area of nanoelectronics and to identify the European specificities and needs.

The FP7 Workshop on Advanced Nanoelectronics Technologies took place on September 11th, 2009, in Brussels, and triggered the participation of a significant number of academics, scientists and engineers actively involved in advanced nanoelectronics R&D.

2. Context

2.1 European Nanoelectronics Landscape

The European nanoelectronics landscape is rich in initiatives and ideas but complex in its coordination, involving a large number of players and domains. Essentially, the FP7 and FP8 ICT is (will be) embedded in a landscape of programmes as e.g. EUREKA/CATRENE, ENIAC, ARTEMIS, FP7 NMP as well as national and regional programmes. Such coordination shall create a common vision on nanoelectronics including short, medium and long term scenarios and priorities, Fig. 2. This shall be followed by the definition of a strategic agenda (like the one defined by ENIAC) and a coordinated implementation of the SRA through calls and the funding of the research projects.

Fig. 3 depicts the European vision of the More Moore and More than Moore domains of nanoelectronics with their main respective drivers: miniaturization and diversification to integrate

functions. Major innovation is achieved via combining System-On-Chip (SoC) and System-In-Package (SiP) in complex systems with high added value. While CATRENE and ENIAC/ARTEMIS are supporting this vision based on their specific research programmes driven by the short-to-medium term R&D priorities of the European industry, it is the FP7 and FP8 mission to connect the Beyond CMOS domain in a pragmatic way with the picture of nanoelectronics research. From Fig. 3 it is clear that the integration of Beyond CMOS technologies into future systems as SoC/SiP becomes urgent in order to take advantage of its high potential in both hybridized-with-CMOS and post-CMOS perspectives. This can be achieved by paying more attention to integrate-ability and system-ability of Beyond CMOS and by a more holistic and multi-disciplinary view linking academics and industry for achieving a critical mass and knowledge in the entire value chain.

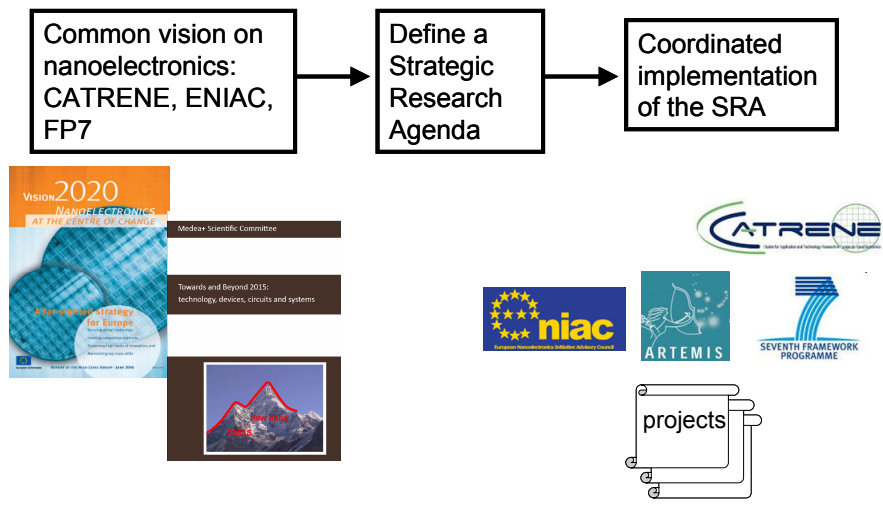


Figure 2: Coordinated implementation of project funding in nanoelectronics domains through CATRENE, ENIAC, ARTEMIS and FP7.

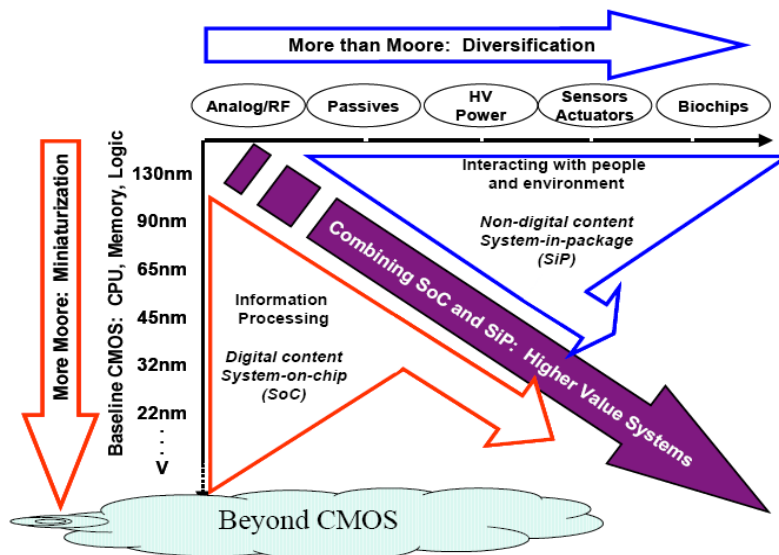


Figure 3: More Moore (MM), More than Moore (MtM) and Beyond CMOS domains of research with miniaturization and diversification drivers for MM and MtM, respectively. The combination of SoC and SiP is expected to result in highly valued systems. To reach and support the SoC/SiP trend, the Beyond CMOS technologies need to meet criteria of integrability and systemability.

A specific feature of Europe is the general commitment to overcome fragmentation in nanoelectronics research, by networking academic research centres and scattered excellence groups through the allocation of additional EU and national funding for coordination and integration of research activities and the mobility of researchers. The EU programmes have pushed the concept of Network of Excellence (NoE) as an effective mechanism, also targeting that their integration effects be extended beyond the end of the initial EU funding.

Another important reality is the evolution of European industry towards fab-less or fab-lite business models (see NXP's strategy) or towards strategic partnerships in which the development of next nano-CMOS technology nodes is foreseen outside Europe (see ST Microelectronics' strategy). The participants of the workshop, in their large majority, have expressed concerns about the impact of such strategies -mainly motivated by economics - and pointed out: (i) the necessity of preserving critical European know-how in the field, (ii) the potential negative impact of such strategies on the research and the high-level education of European electrical engineers specialized in micro/nanoelectronics. On the other hand, it was observed that there is major existing know-how on advanced nano-CMOS technology in research centres like IMEC and CEA-LETI. These centres can offer alternative models for preserving research and know-how in the field. In this context, defining a European-wide strategy for research on Beyond CMOS and More than Moore domains based on the accumulated know-how in More Moore is crucial.

Of course, there are high financial risks related to investing in nanotechnology and Beyond CMOS and it is practically impossible to equally support all the emerging research on materials, devices and architectures in the field. Already, ITRS has considered benchmarking of some of the most promising logic or memory candidates, followed by recommendations and shrinkage of priorities. Next nanoelectronics calls should also smartly consider such approaches by building the future of nanoelectronics on the European strengths existing in the industrial and academic worlds. It is generally accepted that Europe has a high standing in system design and related applications that today are not fully benefiting from the high promise of More than Moore and beyond CMOS. Thus, future developments of system-able and integratable beyond CMOS technologies and their convergence with More than Moore and More Moore technologies in highly reliable SoC/SiP could offer new paths for increased competitiveness and market opportunities.,

2.2 ITRS roadmaps: Emerging Research Devices and Architectures

Undeniably, ITRS¹ is the world reference in nanoelectronics roadmapping and the tremendous work done in the past by the various groups of ITRS served and motivated thousands of engineers to achieve progress in the field. However, the main driving forces of ITRS have been mainly scaling and cost. The figures of merit of any new technology candidate have always been the ones applicable to silicon CMOS. In 2007 ERD-ITRS acknowledged for the first time that **when applying the energy efficiency criterion as a figure of merit for the logic switch, no viable emerging logic technologies appear to have been identified prior to 2007 for information processing beyond CMOS** (more precisely, the switching energy of the beyond CMOS alternatives listed prior to 2007 is not better than the one of ultimate CMOS: $\sim 2 \times 10^{-18}$ J). Thus, a new effort is planned to reshape the beyond CMOS chapter with main focus on the

¹ International Technology Roadmap for Semiconductors, <http://www.itrs.net/>

energy efficiency, the power consumption being considered the most important next driver at both device and system levels.

It is of major importance to mention that all the future developments in Beyond CMOS and More than Moore are foreseen in ITRS as an extended-CMOS vision, see Fig. 4. Thus, **any total disconnection of the nanoelectronics research and funding from the advanced silicon CMOS shall be avoided and could put at very high risk the impact of its results on the applications and markets.**

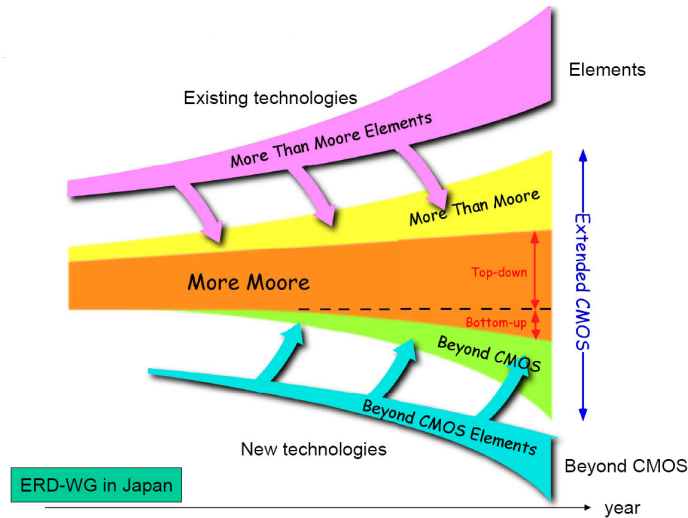


Figure 4: ITRS-ERD vision of the role of Beyond CMOS and More than Moore elements to form future extended CMOS platforms.

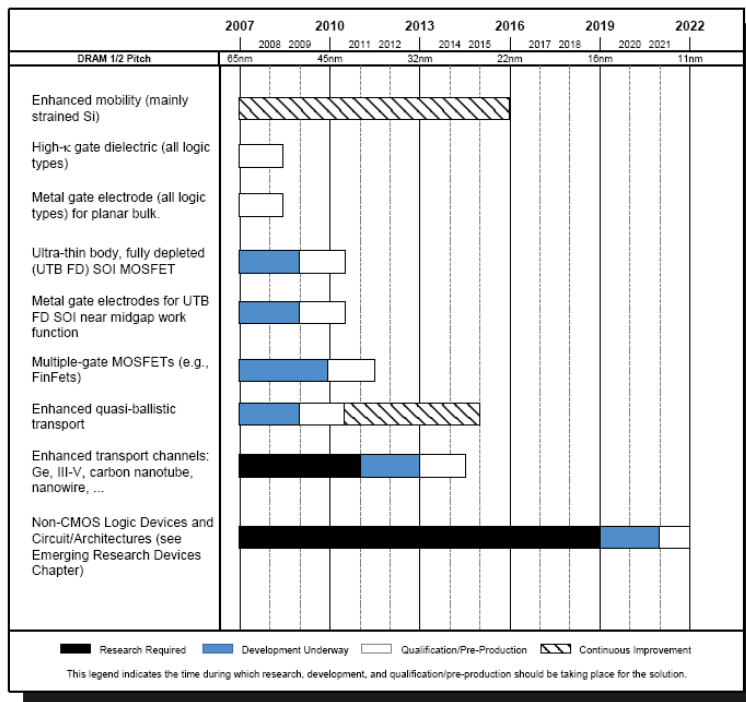


Figure 5: Timeline of research, development, qualification/production and improvements in More Moore devices compared with non-CMOS logic devices and circuit architectures (ERD/ERA). This graph points

out how critical the time frame 2010-2020 is to define a reinforced research and provide major funding on non-CMOS technologies in order to achieve the development phase in 2020-2021. In parallel, there is still needed research in the enhanced transport (novel materials on silicon) part of advanced MOSFETs.

Fig. 5 reports the ITRS research timelines and the maturity of various emerging MOSFET technology boosters (strain, high-k/metal gate, ultra thin body fully depleted SOI, multiple-gates, enhanced transport) versus non-CMOS logic devices and circuit architectures present in the ERD chapter. While for the MOSFET architecture research maturity seems to be achieved in all options – except of enhanced transport channels - to fulfil the needs of the 22nm node by 2016, the picture suggests the necessity of dedicated major research effort on non-CMOS options in the timeframe 2010-2020.

Some of the evaluated emerging architectures by ITRS are shown in Fig. 6 together with the basic computation elements. Here we clearly see the needs of hybridizing silicon with molecular switches, ferromagnetic logic, spin devices and sensors in order to enable heterogeneous and morphic system architectures. For this purpose the integrate-ability of novel technology with CMOS and their reliability become key factors.

Emerging Research Architectures

Architecture	Implementation	Computational Elements	Network	Application
Homogeneous Many-Core	Symmetric cores	CMOS	Irregular/Fixed	Synthesis/GPP
Heterogeneous	Asymmetric cores	CMOS	Irregular/Fixed	Synthesis/GPP
	CMOL	CMOS+Molecular Switches	Irregular/Fixed	Synthesis/GPP
	Molecular Cross-bar	Molecular Switches	Regular/Flexible	Synthesis/GPP
	Check-point	CMOS+ Ferromagnetic logic	Irregular/Fixed	Synthesis/GPP
Morphic	CNN	CMOS+Sensors	Regular/Flexible	Recognition/Vision
	AMP	FG-FET, SET	Irregular/Fixed	Recognition/Vision
	Bio-inspired	MFDI, Spin-gain transistor	Mixed	Recognition Mining Synthesis

Figure 6: The ITRS Emerging Research Architecture section is jointly prepared with Emerging Research Devices; the importance of their interactions will increase in the future. Moreover, according to the reported ITRS table, many of the novel architectures will need the integration of novel materials (molecular, ferromagnetic) and devices (sensors) on silicon CMOS.

3. General R&D Trends and Strategies for Technology-Circuit Interactions

This section summarizes some of the major R&D trends observed in nanoelectronics, as revealed by the workshop presentations but also as reflected in existing technical literature, international

scientific reports (such as ITRS, ENIAC SRA) and industry roadmaps. These trends are categorized in system, device and material perspectives but it is obvious that these three levels are highly interactive and cannot be artificially separated.

3.1 R&D Trends

Trends in System Perspectives:

- Novel functionality (sensing, energy scavenging and communication layers together with computation) by heterogeneous integration
- Extending Moore's law in 3D;
- Energy efficient design (reversible, adiabatic, bio-inspired);
- Ultra low power design techniques;
- Zero-power concepts (zero-power standby PC);
- High reliability;
- System miniaturization continued;
- Thermal aware design.

Trends in Device & Technology Perspectives:

- Evaluation of how far a device/technology operates from fundamental limits;
- Miniaturization continued but facing huge challenges;
- 22nm CMOS by 2016;
- Energy dissipation per circuit element or per bit decreasing (CMOS: $\sim 1000kT$).
- Energy efficient switch (steep subthreshold switches);
- System-able nano-devices;
- Reliability and variability;
- Convergence of front-end and back-end (packaging) technologies.

Trends in Materials Perspectives:

- Novel materials for extending CMOS and their manufacturability:
 - III-V compounds, Ge;
 - Schottky contacts
 - Ultra thin films on insulators
 - New gate stacks
 - Alternative S/D contacting techniques
 - Nanowires
 - Carbon electronics as alternative to silicon (graphene and CNTs);
 - Materials to extend interconnects
 - Materials for advanced processing (lithography)
- Materials for beyond CMOS (logic and memory): Ferromagnetic Materials, Complex oxides, Strongly Correlated Electron State Materials, Novel Molecules;
- Novel materials for solid state lighting;
- Novel materials for nano-packaging.

Of major importance and common to all levels are the concepts of "**systemability**", "**manufacturability**", "**integratability**" to achieve a full electronic system. While the last two terms are more common and clear, the systemability needs particular attention and explanations.

The **systemability criteria** of novel devices/technologies have been discussed in the past by Hugo De Man and detailed in the MEDEA+ report 'Towards and beyond 2015: technology, devices, circuits and systems'. In general, a novel device technology is considered to be systemable if it features the following properties:

- Ability to co-host/co-integrate three basic system functionalities: computation, storage and communication (interconnects);
- For each type of function (digital computation, storage, etc.) there are particular systemability sub-criteria: For instance, building binary logic circuits and systems requires from a novel switch architecture to fulfil the following criteria:
 - Inversion, flexibility and logical completeness;
 - Isolation (output does not affect input);
 - Logic gain (output may drive more than one following gate and a High Ion/Ioff Ratio);
 - Self Restoring / Stable (Signal quality restored in each gate);
 - Low cost manufacturability;
 - Reliability (aging, wear-out, radiation immunity);
 - Performance (transaction throughput improvement);
 - "Span of Control" is an important means of connecting device performance and area to communication performance, relating time to space; the metric measures how other devices may be contacted within a characteristic delay of the switch being dependent not only on switch delay, but switch area as well as communication speed.
- Power density and/or energy consumption of the three system functionalities and their balance;
- Room temperature operation for computation and storage: it is very important that new nano-devices operate at room temperature if systems that use them are to be embedded in everyday items;
- Device variability and cost-effective solutions in order to build reliable systems from failure prone components with a given defect density and subject to increased soft error rates (fault tolerant design);
- Fundamental lower limits of logic and digital architectures as a function of the device, technology and architecture.
- Possibility of building analogue or mixed-signal systems from new devices, because in many cases new systems will have to interface to the analogue world.
- Adequate reliability and yield must be adequate for proposed applications.
- Added value with respect to the best silicon solutions that will be achievable at the end of CMOS scaling; essentially the potential to develop new functionalities other than computing (e.g. sensing, actuating) that could lead to more rewarding applications for nanotechnology than simply trying to beat ultimate CMOS on computing functions.

3.2 Strategies for Increased Technology – Design Interactions

In many of the workshop presentations the importance of a strategy for increasing the interaction between technology and system design has been systematically mentioned. One such possibility

is reported in Fig. 7, which proposes an approach of co-optimizing the technology and the design from the very beginning up to the product prototyping and process qualification. While FP7/FP8 calls do not support the design or qualification of full products, the importance of Fig. 7 is related to the proposed exploration of design and architecture possibilities that leverage a technology opportunity in an interactive mode. Such a strategy has the advantage of addressing the risks concerns for product groups at a very early stage and account for all supply chain partners and their constraints.

It is believed that future successful FP7/FP8 proposals should trigger system-level innovation based on novel system-able technologies and devices by proposing such application focused approaches based on narrowing the gap between design and technology.

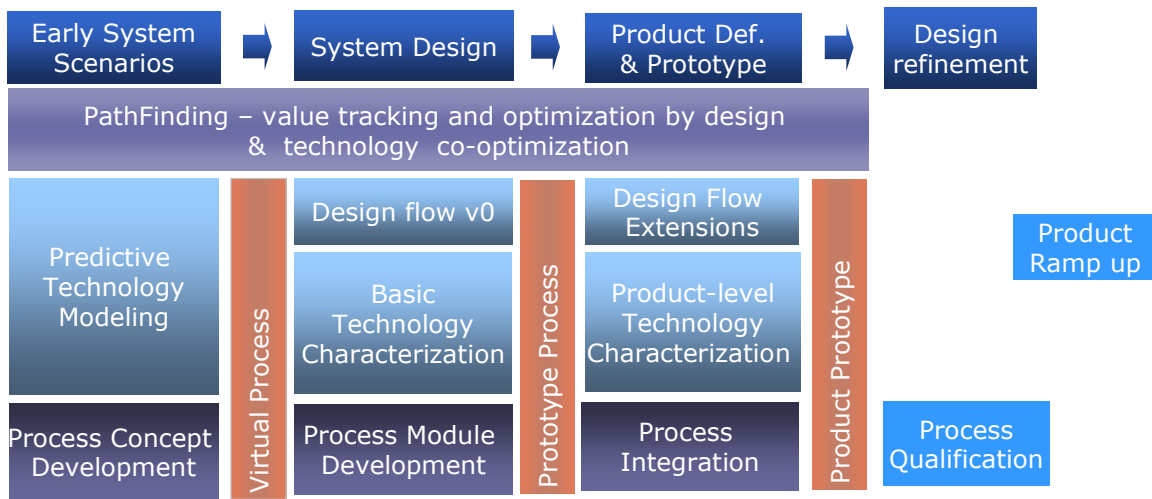


Figure 7: Possible approach for technology-design interactive exploration from a very early stage.

4. Very Advanced CMOS and System Design

Today silicon nano-CMOS is a mature technology supporting high performance electronic products by the performance of advanced technology nodes (with the 22nm node projected to be available by 2016). Despite the fact that the access to nano-CMOS experimental devices from industry is more and more difficult for academic partners, Europe has the advantage of having two large nano-CMOS research platforms in IMEC and CEA-LETI that could continue to play a significant role in the field. Fraunhofer and Tyndall are also major contributors to the field of advanced silicon nano-scale technologies.

The discussion at the workshop highlighted the importance of nano-CMOS as the true supporting technology for very high performance electronic systems. Thus, maximizing the use and integration of More Moore in advance electronic system needs to continue and the novel system design should take into account the challenges of nano-CMOS: variability, power density, leakage power, etc. Again, the FP7/FP8 programmes do not support R&D on the final products (such as PDA's or other similar ones), they are ending at the SoC or SiP levels. However, the wanted characteristics of a final product can be used to derive target performance at circuit and device levels.

It is considered of strategic importance to preserve and continue developing CMOS expertise in Europe. The main reasons for such choice are:

- **Future technology appropriation** – keeping research activities on nano-CMOS technology in large research institutes on (n+2) and (n+3) technology nodes and in universities on (n+4) nodes is important for seizing coming opportunities on a global market;
- **Preserve Europe's attractiveness for production** – despite the present economic context, it is believed that preserving high level CMOS technology expertise in Europe will enable future production implantation in Europe (based on the example of Global Foundries in Dresden);
- **Enable innovation in electronic systems** design and hardware combining MM and MtM;
- **Maintain high level trainings and university curricula** on advanced CMOS topics;
- **Prepare the path for future Beyond-CMOS** device and circuit architectures that will be co-integrated on CMOS platforms.

The challenges related to the future extensions of silicon CMOS technology are considered of high importance and involve combined circuit-technology solutions on the following topics.

- Circuit design view
 - Power dissipation constraints;
 - SRAM stability;
 - Analogue design challenges;
 - Device variability and model accuracy;
 - Design methodology and tools;
 - Reliability.
- Technology view:
 - Device leakage current and growing power dissipation;
 - Increased process variability.

The European academic research activities on the characterization, modelling and simulation of nano-CMOS are extremely strong and internationally recognized, often representing the international state-of-the-art. Europe has also significant expertise, big facilities and strong suppliers in physical characterization that should be further developed. Models based on high levels of abstraction cannot be developed without the understanding of the device physics and the development of physical analytical models. Moreover, the analogue design and mixed-mode system design with advanced CMOS critically need advanced modelling and simulation.

Many challenges are identified in the simulation of nano-CMOS and should be addressed in the future by the European research community:

- Multi-physics and multi-scale/hierarchical modelling methodologies;
- Quantum transport;
- Semiclassical transport (Multi-subband);
- MC calibrated deterministic transport models;
- Compact models including quasi-ballistic, quantum and atomic scale effects;
- Account for: holes, thermo electro-mechanical effects, BTB tunnelling, variability;
- Process modelling for new materials and device architectures.

5. Beyond CMOS

The scientific and technical expectations for Beyond CMOS devices and circuit/system architectures are extremely high. They are essentially related to the **ultra low power and novel functionalities** demands that silicon CMOS is not able to deliver today.

In a first phase, the **integration of Beyond CMOS in advanced** (and possibly conventional) **CMOS for use in advanced electronic system will enable earlier introduction** (before 2020) **and impact**.

One key topic in beyond CMOS is the quest for the new switch; this is an activity also strongly supported by the Nanoelectronics Research Initiative (NRI) in US. One of the missions of NRI in this respect is to demonstrate novel computing devices capable of replacing the CMOS FET as a logic switch in the 2020 timeframe.

These devices should show significant advantage over ultimate MOSFETs in power, performance, density and cost to enable the semiconductor industry to extend the historical cost and performance trends for information technology. For this purpose, NRI defined five research vectors, focused on discovering and demonstrating new devices and circuit elements for doing computation.

The required characteristics of the new switch are: scalability, performance, energy efficiency, gain, operational reliability and room temperature operation. NRI also mentions that the preferred approach will include CMOS process compatibility and CMOS architectural compatibility.

The primary research vectors defined by NRI are:

- NEW DEVICE – with alternative state vector (spin, phase, magnetic flux quanta, mechanical deformation, dipole orientation, molecular state);
- NEW WAYS TO CONNECT DEVICES – including non-charge data transfer;
- NEW METHODS FOR COMPUTATION – including non-equilibrium systems;
- NEW METHODS TO MANAGE HEAT – focused on nanoscale phonon engineering;
- NEW METHODS OF FABRICATION –focused on direct self-assembly.

The workshop highlighted the importance of **dedicated focused research and funding for the novel switch in the context of the low power driver and the systemability criteria**. Particular attention should be given to novel device architectures such as **the junction-less FETs and steep subthreshold slope transistors** (particularly, the tunnel FET devices) that can be integrated on the advanced CMOS platforms by exploiting ultra-thin films, nanowire structures and/or appropriate materials (III-V, graphene) offering band-gap engineering opportunities. The engineering and exploitation of novel switches in appropriate low voltage low power circuit architectures and complex energy efficient systems is one of the great challenges for Beyond CMOS.

Today, the challenges are the fabrication of ever smaller and faster devices coupled with a reduction of power consumption. The key element for this is low-voltage operation, because power consumption of a circuit is proportional to the square of the supply voltage.

European research has traditionally been very creative in the field of microelectronics. For instance, most innovations in silicon-on-insulator (SOI) technology were made in Europe in the 80's and 90's by CEA-LETI, IMEC, Philips, etc. The payback for European industry was the

establishment of SOITEC and the mass production of SOI chips by EM Microelectronic-Marlin SA, AMD-Dresden and Philips NXP. This has allowed Europe to position itself in unique niches such as the production of mixed-signal circuits that operate at 0.5-V implemented on a fully depleted silicon-on-insulator substrate by EM Microelectronic-Marlin SA, making this company a world-leading specialist in low-power process technology. In a similar way, SOI technology has enabled Philips NXP to become the exclusive manufacturer of extremely high-quality class D audio amplifiers.

Novel devices are emerging from European research centres. The junctionless transistor, for instance, is an SOI nanowire transistor that does not require the formation of junctions. This greatly simplifies the fabrication process and allows to fabricate shorter channel devices than standard CMOS. Such devices have an on/off current ratio better than 10^6 for a supply voltage of only 0.5V, which is significantly better than standard CMOS and allows for low-voltage, low-power operation. Achieving a high on/off current ratio for lower supply voltages necessitates the development of devices based on quantum tunnelling effects, and possibly materials other than silicon. These devices, called “steep subthreshold slope transistors” (S3T), have become the “holy grail” of the micro/nanoelectronics industry. Europe happens to be at the forefront of S3T technology, but massive DARPA investments in S3T in the USA threaten European leadership.

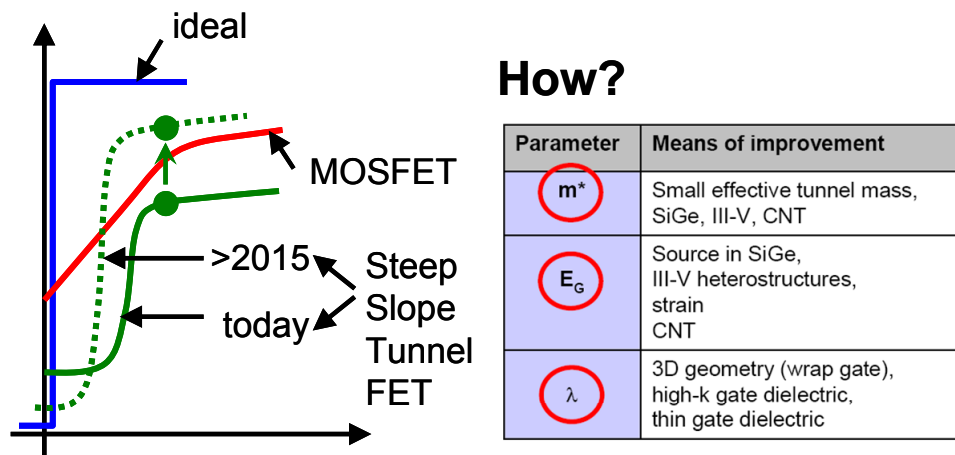


Figure 8: Expected performance improvements for the next Beyond CMOS switch (like Tunnel FETs): steep transition between off and on states enabling low voltage operation and low subthreshold leakage.

Other important research directions in Beyond CMOS concern:

- **Emerging memories** targeting the concept of non-volatile **universal memory**.

Several concepts have emerged in recent years which are based on ions/atoms as state variable instead of the electron charge in conventional electronics. Because of their large mass and their capability to get latched into positions of the crystal lattice, these ions/atoms can be favorably exploited for novel non-volatile memory devices, the so-called nano-ionic and nano-thermal memories. These are two-terminal devices in which the resistance is changed hysteretically by electrical stimulation (resistive memories, RRAM). Nano-ionic memories come in different variants, electro-chemical metallization memories (ECM) and valence change memories (VCM). Nano-thermal memories are,

e.g., nanowire phase-change memories or thermo-chemical (fuse-antifuse) memories. Compared to Flash, RRAM show several advantages. Typically, they exhibit fast write/erase cycles < 100 ns, endurance $> 10^7$ write/erase cycles, and low write/erase voltages < 5 V (< 1.5 V for some ECM types). In addition a minimum features size F of approx. 5 nm is predicted for several RRAM concepts, well below the expected minimum F for Flash. Furthermore, RRAM can exploit the $4 F^2$ cell concepts as well as 3-D stacking approaches, so that Tbit/cm² densities become a realistic vision.

Memory architectures

RRAM cells can be arranged in passive matrices which are particularly dense and can possibly be produced cost-effectively. Because such passive crossbar arrays of resistive switches can be employed as programmable logic arrays, RRAMs are highly interesting as an alternative to conventional CMOS based processors which use architectures derived from the von Neumann concept. The ultra-high cell density as well as the local fusion of memory and logic (avoiding the energy consuming data transfer across the chip for feeding the arithmetic and floating point units) may lead to systems which are much more energy efficient than current solutions. In addition, a defect tolerance can easily be built-in. If stable multi-level RRAM concepts can be realized, a completely new generation of artificial neural networks will be feasible. Most probably, all these concepts will be hybrid solutions based on a CMOS platform for signal amplification and interaction with the chip periphery

- **Nanoscale thermal processes:** noise, reduced heat transport, phase control, e.g., physics of phonons;
- **Nanophotonic technologies** for device and/or interconnect functions. In particular, the convergence between nanoelectronics and photonics has attracted increased interest, including joint road-mapping² to 2020 and beyond. The efficient design of intra- and inter-chip communication is key to the success of future multi-core processors. Photonic Networks-On-Chip offer a unique solution for high performance embedded computing in terms of combined ultra-high bandwidth and limited energy dissipation. Inter-chip optical interconnections are expected to provide high-speed and large-capacity bus lines connecting spatially separated LSI chips on a printed circuit board.

Finally, it was concluded that the **FP7/FP8 calls on Beyond CMOS domain can be easily differentiated from the calls and funding in ENIAC and CATRENE**. A list of identified topics (key words) reflecting the workshop presentations is summarized here:

- Co-integration of beyond CMOS and silicon CMOS (for quick industrial acceptance);
- Challenges in extending CMOS technology: power dissipation and variability;
- Energy efficient devices, circuits and systems;
- More functionality for information processing, more application specific under reliability constraints;
- Multi-scale simulation and modelling and new design concepts;
- Nanoelectronics-photonics convergence (including electro-optical simulation, new design and technology concepts);
- Carbon and molecular electronics;
- Non-Volatile Terabit memory technology;

² Communications Technology Roadmap, <http://mph-roadmap.mit.edu>.

- Understand fundamental artefacts and limits of nano;
- Computational material and device science;
- Nanoscale manufacturing;
- Nano for multi-mode, multi-band Radio Frequency ICs (as convergence between Beyond CMOS and MtM).

6. Advanced More than Moore Nanoelectronics

The More Than Moore (MtM) domain is considered of highest strategic importance for the European industries and could constitute the final complex system platform for combining More Moore and Beyond CMOS technologies with other functionalities offered by the MtM devices. Therefore, the heterogeneous integration of various functional layers with optimized and diverse technologies (logic, memory, analogue, energy and power management, sensing, communications) could enable solutions for multi-functional systems needed in future nanoelectronics.

The FP7/FP8 calls will not include advancements in nanosensors, nanoactuators or related materials themselves, but rather their use and integration in combination with advanced nanoelectronics (e.g. in a 3D context).

A summary of the R&D future directions and priorities for MtM nanoelectronics is presented below being organized in three major directions: (i) specific MtM design-technology interactions, (ii) novel functionality of CMOS, (iii) essential future technologies for MtM heterogeneous integration.

Specific MtM design-technology interactions:

- Design and fabrication of energy autonomous systems with focus on sub-100 μ W systems, as technology-system interaction enabling future Wireless Sensor Networks (WSN) for ambient intelligence applications;
- Design methodologies that balance benefits of integrating some MtM functions on a chip versus other functions in the package;
- 3D system integration and packaging.

Novel functionality on CMOS:

- Energy storage to CMOS;
- Microfluidic on CMOS;
- Nanostructures for sensing on CMOS;
- Biosensor integration on CMOS.

Essential future technologies for MtM heterogeneous integration:

- Radiofrequency technologies;
- High voltage and power technologies;
- Solid state lightening technology;
- Front-end and back-end convergence;
- Plastic and organic electronics;
- Convergence of photonics and electronics through heterogeneous integration.

7. Drivers of Future Nanoelectronics Research

The past main drivers of nanoelectronics have been the cost and the aggressive miniaturization of the switching element that have been translated in a more than 40 years-long success story by the silicon CMOS technology and supported computing and communication applications.

At the workshop it was pointed out that in the future we will move to the **ultra low power nanoelectronics era**. There **novel functionalities** will be offered by **energy efficient design and technologies** for still **miniaturized and highly reliable systems**, taking into account **cost constraints**. These are expected to be extraordinary new challenges for research and development.

Therefore, future drivers of nanoelectronics are much more complex and should be addressed in a more holistic way, simultaneously considering:

- **System miniaturization and integration** for mobile computing, communication and sensing;
- **Reduction of power consumption via energy efficient system design and novel devices**;
- **Extended functionality and enhanced performance**;
- **Strategies for early risk concerns and more product focus** - the full supply chain shall be considered for each new nanotechnology or device candidate;
- **Societal and economical impacts**. The societal needs should be translated into future applications and markets for nanoelectronics. In Europe, the following application domains are considered highly relevant and important:
 - Health care and wellness (address the needs of the ageing society)
 - Transport and mobility
 - Energy and environment
 - Communications and infotainment
 - Security and safety

8. Recommendations to the WP 2011-13

One of the goals of the workshop was to organize a brainstorming session, following the various technical presentations and devise some useful recommendations emerging from the various expressed positions. This section details the results of this process.

Some general research directions and priorities in nanoelectronics are recommended for future support in FP7/FP8 calls:

- Address the full nanoelectronics chain from technology to packaged systems; improved synergy and interactions between technology, design and applications.
- Address the constraints for applicability of novel technologies/devices: systemability, co-exploration of architecture and technology from the first day, concepts for design flow and reliability; position with respect to fundamental limits of computation.
- Devices supplementing CMOS, adding new functionality to CMOS (including sensor integration) in a cost-effective way.

- Technologies, devices, design for ultra-low power era; energy efficient devices and circuits compatible with scaling.
- Concepts and technologies for next switches: sub-kT/q device concepts; scaling and integration with CMOS.

The various discussions around these topics are summarized in five main recommendations:

Recommendation 1:

Information processing to accomplish specific system functions requires several different interactive layers. Taxonomy of these layers to further distinguish their roles has been proposed by the Emerging Research Devices Group of ITRS and includes: (1) State Variables, (2) Material, (3) Device, (4) Data Representation and (5) Architecture (see Fig. 9). The workshop group believes that there is a stringent need **to define calls for future transversal research projects** addressing in an integrated way these layers. We recommend two possible approaches for the future nanoelectronics FP7/FP8 calls to comply with this observation:

- Stimulate, organize and fund **clusters of complementary small projects** (STREP like) grouped in sub-programmes with headings that can stimulate advanced system thinking and favour multi-disciplinary cooperation. Some concrete mechanisms to stimulate a real multi-disciplinary cooperation around a problem-solving approach in a cluster should be identified;
- Stimulate, organize and fund **large multi-disciplinary programmes** (Integrated Project like) addressing nanoelectronics research in an integrated (holistic) manner and guided by more system level thinking and having a long term vision.

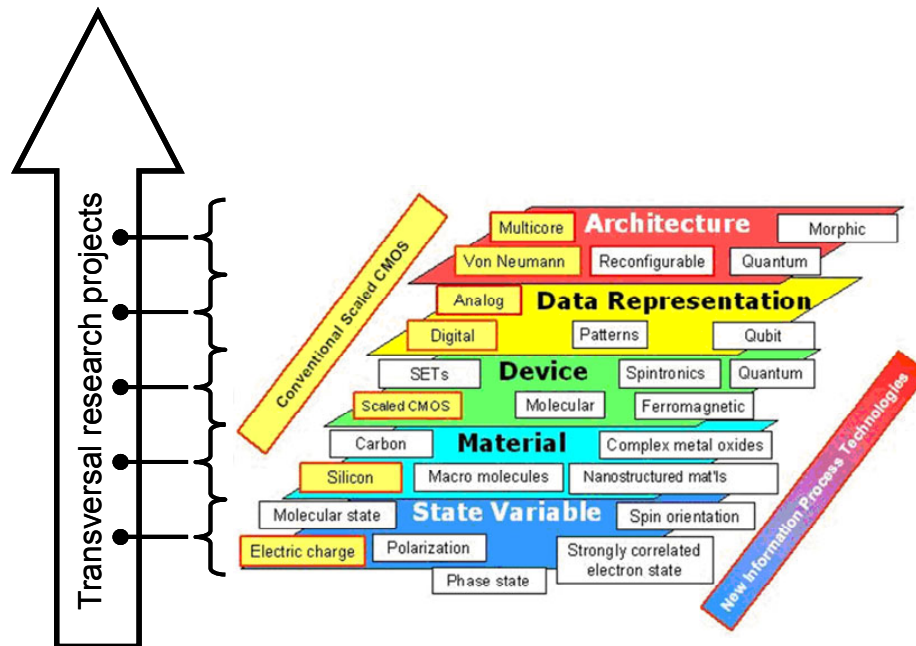


Figure 9: Illustration of the components needed in future transversal research projects.

Recommendation 2:

Beyond CMOS and More than Moore domains of nanoelectronics are of great importance for Europe. We have strong academic communities and industries with relevant activities that can benefit from more investments in this domain. An important remark is that scaling, while still of major interest is not the only driver of these two domains. However, co-integration with CMOS is seen as a major advantage. Thus, we recommend **to define major nanoelectronics calls in Beyond CMOS and More than Moore domains** that share the following features:

- energy efficiency (low power), system-ability and novel functionality replace scaling as major drivers to prioritize for the future nanoelectronics research and developments (nano-scaling preserves its high importance but is not the primary factor for innovation and progress on future nanoelectronics roadmaps);
- in a first phase, the technologies and devices developed in Beyond CMOS and More than Moore should supplement CMOS;
- in second phase, mature (system-able) Beyond CMOS technologies (nanoscale manufacturable) can completely replace CMOS for some particular (energy efficient) applications;
- the convergence of Beyond CMOS and More than Moore should be stimulated;
- performance challenges should be included and addressed at all hierarchical levels;
- design challenges should be included and addressed at all hierarchical levels.

Recommendation 3:

We recommend **preserving some small-to-medium size focused research projects on a single layer of taxonomy, but any project of such type should be defined in a system integration perspective** and offer clear visions of achievable device and system performance boosting.

Some of the potential topics of interest recommended for focused research projects with system integration potential are listed in sections "Beyond CMOS" and "Advanced More than Moore Nanoelectronics". Additionally, it is recommended that such focused projects shall be aligned with some of the future drivers of nanoelectronics as presented in section 7.

Recommendation 4:

The contributors highlighted the importance of other **key topics to be prioritized in future nanoelectronics calls such as: reliability, 3D integration, heterogeneous integration and packaging** as major domains of interest for R&D in Europe.

The reliability aspects must be considered at technology, device and system levels and are one of the criteria for the system-ability potential of new technology. Future reliability considerations of beyond CMOS technologies should also include the related variability.

Recommendation 5:

The participants highlighted the strategic importance of preserving know-how in Europe on advanced CMOS technology and devices, despite the existing trends of many companies to go fabless or fablite and/or concentrate on other technology options.

There are strong European academic research communities with strong background in advanced CMOS modelling and characterization and two state-of-the-art research platforms (IMEC and CEA-LETI) where Europe has significant accumulated know-how in nano-CMOS. It is recommended to preserve some selected topics in future calls in this domain, particularly focused **to sustain nano-CMOS research on: (i) advanced design-technology solutions for power consumption, variability and thermal issues, (ii) partitioning challenges: scaling analogue or moving large parts to digital and (iii) novel materials and equipments.**

It is particularly recommended **to explore the CMOS science and technology aspects for n+4 technology nodes and beyond** for understanding new physical phenomena, studying and validating new concepts, novel materials and non-standard processing. The universities should work closely together with large European research institutes offering access for validations on their advanced CMOS platforms and with industries that can seize novel opportunities in technology and CMOS advanced design. There is an identified need to regularly assess that there is no technology gap building-up between the applied research programmes (CATRENE and ENIAC) and the FP7/FP8 research programmes.

Annex 1:

Application scenarios: *How could economy and society benefit more from advances in nanoelectronics?*

Guardian Angel (GA) for aged people

By J.P. Colinge

The Guardian Angel (GA) is a device helping old people with their main problems: loss of memory, loneliness, reduced mobility, e.g. losing their glasses and keys, having nobody to talk to and feeling useless in society. It will also help to monitor their medical condition and call help if necessary.

It would consist of a fixed internet connection with flat screen and audio interface, no keyboard, a voice-controlled interface, and a wearable iPod-size device (call it the Guardian Angel, GA) that is connected to the main system. The person wears the GA at all times. Using RFID, the system can locate the glasses, keys, and other objects in the house. So, by saying “where are my glasses”, the GA would reply “they are on the kitchen table”. The system would have Skype-like connection to friends, family and networks of old people. They can also play games such as Scrabble, chess, etc. For using the system, voluntary, paid or unpaid jobs such as helping kids with homework or translation jobs could be offered on-line to the old persons. The GA is the voice interface. It contains a loudspeaker and a small display, but all the processing is done in the bigger fixed internet connection computer.

The medical surveillance role of the GA includes a fall sensor and basic medical monitoring, with data transmitted to a watch centre.

For the very lonely ones, one could recreate a virtual ex-wife or ex-husband or lost child on the display. After all, many kids live part of their life in virtual worlds on the internet and feel happy there. For elderly this is a role usually held by a dog or a cat.

Of course, a lot of vultures will be attracted by such a system and will try to hack the system to take advantage of the elderly and steal their money (this already happens in present homes for the elderly too frequently, unfortunately). So, efficient security techniques should be used.

Technologies required by Guardian Angels:

- **RF ID sensor technologies to locate lost glasses or keys and translate the sensed result into a sentence such as “your keys are on the kitchen table”;**
- **Wearable health monitor with body area sensor networks;**
- **Very high bandwidth internet connections;**
- **Recharging the GA batteries in a “wireless” manner;**
- **3D virtual “holographic” companions.**

Autonomous Robots

By Rainer Waser

Among future nanoelectronics scenarios, the vision of autonomous robots is probably the scenario with the largest societal impact. Autonomous robots will stand as intelligent machines capable of performing tasks in the world by themselves, without explicit human control. The underlying technology needed for building autonomous robots includes control, architectures, learning, manipulation, grasping, navigation and mapping, altogether requiring tremendous innovation at system and hardware levels. Finally, the living systems can be considered the prototypes of autonomous systems.

Completely new industries will arise, comparable in size to the automobile industry today. Europe with its strength in mechanical engineering, process engineering, electronics (including sensors and actuators) has got the chance to be in the fore-front of such a development, if it takes the chance without hesitation.

Real-world environments such as family households are highly dynamical, with new unknown objects appearing frequently. Autonomous robots would need to move and work in such environment, would need to be self-sufficient to a certain degree, and to interact with humans in a human-like fashion. In particular, these systems will require a pronounced capability of self-learning. In order to realize such systems a computational power is needed which exceeds large PC clusters of today and shows energy efficiency well beyond current technology.

Technologies required for Autonomous Robots:

- **Heterogeneous integration of nanosensors and actuators with computational electronics;**
- **Ultra low power miniaturized processor technologies; the resistive crossbar architectures may supply a processor technology which will fulfil these requirements;**
- **Software-hardware co-design;**
- **Highly reliable system design;**
- **Convergence of SoC and SiP;**
- **Advanced packaging techniques;**
- **Advanced power management and novel energy storage technology.**

Ubiquitous powering: Energy Aware Nanoelectronic Companions

By Adrian Ionescu

A ubiquitously powered computational and communication system is the result of convergence between zero-standby power mobile computing and mobile communications enabled by convergence of More Moore, Beyond CMOS and More than Moore, including thin film battery technology and multi-scavenger heterogeneous integration.

*Ubiquitous powering of systems will feature zero standby power with novel steep slope switch and memory technology and have energy consumption and efficiency during computational and communication activities closer to the ones of biological systems. They will be designed based on bio-inspired power management and energy storage, being able to automatically switch between standby mode (**SLEEP**), scavenging and communication modes according to the dynamic environment.*

*Ubiquitous powering devices will not need any battery replacement during their lifetime and will exploit novel thin film batteries, fully integrated in the system. These batteries will recharge via energy harvesting (**EAT**) interfaces by smartly detecting in the environment the energy, which will be used as food by the system. The system will activate the most efficient energy harvester depending on the available sources of energy in the close environment (indoor and outdoor).*

*Ubiquitously powered systems will be able to communicate (**TALK**) to each other, connect their users to each other and/or make wireless connections via internet to retrieve usual information needed by their users. They will be able to emit warnings, advices and, in extreme cases, take limited informational decisions (**THINK** and **ACT**) related to the user's safety and needs.*

Technologies required by Ubiquitous Powering:

- **Energy efficient system-technology co-design approach to reach near-biological efficiency (bio-inspired power management);**
- **Energy efficient logic and memory (more than 2 decades better than CMOS);**
- **3D integratable thin film battery on CMOS;**
- **Heterogeneous integration of multi-scavenging techniques;**
- **System reconfigurability;**
- **3D integrated RF-front ends;**
- **Convergence of SoC and SiP;**
- **Integrated nanosensors and actuators;**
- **Integrated laser sources for projectable interfaces;**
- **Miniaturized and highly reliable heterogeneous integration;**
- **Self-repairing and high redundancy functions.**

The "All-in-One" device

By Reinhard Mahnkopf

For future communication there will be sooner or later just one portable device which allows connection, communication, information exchange basically everywhere and to/from everyone: It will be able to manage video and music down streaming with ultra high data rate, it will allow multi-partner online gaming, of course optimum internet access, and it will serve all relevant applications you can think of (or maybe not yet). It will provide connectivity in every kind, cellular, WLAN, GPS, FM radio, etc. It will be extremely user-friendly, with a nice touch screen and a bigger display than we are used to today. More and more functionalities will be added over time, at least for high-end smart "phones". LTE and LTE advanced standards will be used.

Since cost will be the key subject for this device as for all consumer devices, the future underlying process technology needs to be CMOS compatible to be able to take advantage of high volume Si processing and manufacturing.

All these features require very low power technologies: power consumption of future transistors will have to be decreased further and further while the dynamic performance needs to be kept at least at the same level as it is today. At the same time more and more content will be integrated on fewer chips, so the process technology will have to deal not just with digital information processing, but with storing information, with power amplification, and with interfacing with the outside world. Future transistors should provide excellent RF/MS capability in addition. But key enabler will be the ultra low power consumption of future transistor concepts which allows the all-in-one device to be operated with long standby or in active modes for long times.

Technologies required by All-in-One devices:

- **very low power technologies, for logic & memory, for standby and active mode;**
- **advanced low power circuitry / system power management;**
- **very high bandwidth internet connections;**
- **RF high data band width / mm wave transmission;**
- **heterogeneous integration of multiple chips with different functionalities;**
- **advanced packaging techniques / potential convergence of SoC and SiP;**
- **CMOS image sensors, other integrated sensors & actuators;**
- **display/touch-screen technologies.**

Autonomous City Mobility Environment (ACME)

By Livio Baldi

A new public transportation system in big cities to complement rail systems in a flexible way

It is based on a fleet of small electrical cars provided with autonomous navigation system, integrated in a city network. Cars are booked through cell phone messages to a central system (it could be used also for billing), that verifies availability and sends confirmation and scheduled arrival time. Several passengers can be accommodated in a single car by automatic planning. Solar roofs on cars and car parking stations can be used to reduce dependence from the electrical grid. Car allocation to different areas of the city is dependent on the concentration of potential users and is based on the analysis of a cell phone network.

Technologies required by ACME:

- **electrical cars: power electronics, smart power, batteries, super-capacitors, photovoltaics;**
- **autonomous cars: sensors arrays, radar optical, infrared, navigation systems, real time image recognition, powerful computers for real time collision avoidance programmes, RF car-to-car communications;**
- **Control system: integrated network of sensors to assess traffic density, powerful computers (perhaps quantum) for real time requirement analysis and traffic flow optimization;**
- **Collateral big parking places at the city borders for “stupid” cars.**