SiNANO INSTITUTE

SINANO Institute vision - *June 2009*

This document is devoted to the Sinano Institute vision in the *More Moore, More than Moore and Beyond-CMOS* domains.

Name of contributors:

Asen Asenov	David Leadley
Francis Balestra	Siegfried Mantl
Thierry Baron	Bernd Meinerzhagen
Jean-Pierre Colinge	Florian Merget
Nick Cowern	Mireille Mouis
Sorin Cristoloveanu	Androula Nassiopoulou
Emmanuel Dubois	Sarah Olsen
Olof Engström	Anthony O'Neill
David Esseni	Mikael Ostling
Denis Flandre	M. Otto
Francisco Gamiz	Marco Pala
Gerard Ghibaudo	Evan Parker
Steve Hall	Jean-Pierre Raskin
Paul Hurley	Enrico Sangiorgi
Giuseppe Iannaccone	Andreas Schenk
Benjamin Iniguez	Luca Selmi,
Erich Kasper	Bernd Spangenberg
Valeria Kilchytska	Marco Tartagni
Heinrich Kurz	Alex Zaslawsky

Table of Contents

EXECUTIVE SUMMARY

The SiNANO Institute has engaged its leading thinkers to produce its vision in the nano-electronics field through the next two decades. The view is clear – there is nothing on the horizon to rival silicon-based CMOS. With innovation and ingenuity the technology with go on and on. Novel materials, innovative devices in the More than Moore and beyond-CMOS domains will also be integrated on CMOS platforms in order to add functionalities and overcome some possible limitations of CMOS at the end of the roadmap. There is incredible opportunity not only for technological advancement but for dramatically extending the reach and impact of this technology on our society. In this first statement we set out the challenges that we consider European community should be taking on. There is a critical requirement to work alongside other disciplines particularly biological and environmental to fulfill this fantastic potential. These are very exciting times and the SiNANO Institute is set to play a pivotal role in steering and driving forward research to ensure Europe maintains its focus in this new nano age.

1. Introduction

The minimum critical feature size of the elementary nanoelectronic devices (physical gate length of the transistors) will drop from 25nm in 2007 (65nm technology node) to about 4.5nm in 2022 (11nm node). In the sub-10nm range, "Beyond-CMOS" devices, based on nanowires, nanodots, carbon electronics or other nanodevices, will certainly play an important role and could be integrated on CMOS platforms in order to pursue integration down to nanometre structures. Si will remain the main semiconductor material for the foreseeable future, but the required performance improvements for the end of the roadmap for high performance, low and ultra low power applications will lead to a substantial enlargement of the number of new materials, technologies and device architectures.

Therefore, new generations of Nanoelectronic ICs present increasingly formidable multidisciplinary challenges at the most fundamental level (novel materials, new physical phenomena, ultimate technological processes, etc.). This long term research must be supported now in order to prepare the path for future nanoelectronic technologies, as a 15-to-20 years time frame is usually necessary between the first validation of a new innovative idea and its full demonstration and acceptance into complex systems.

In this timeframe, performance will also derive from heterogeneity, referring to the increasing diversity of functions integrated on to CMOS platforms as envisaged in the "More than Moore" approach. Again, to learn how to combine and integrate CMOS with sensors, actuators, MEMS, NEMS, RF components, photonics and biochips and demonstrate their innovative benefits requires enhancing multi-disciplinary scientific experiments, from design to fabrication and characterization, by a large research community.

Europe needs to cover the whole research area underpinning this fundamental technology for the economy of the next decades, recognising that today, 16% of the world economy is built

on electronics products and related services: communication, computing, consumer electronics, health, transport, security, environment, etc. This percentage is growing every year.

2. Advancing core technology for CMOS and memories

Context:
Our primary observation is that there is nothing on the horizon to replace extremely scaled, silicon-based CMOS for the next 20 years, at least, as the technology that underpins ICT and hence all aspects of modern life. Whilst scaling will continue to be a driver, possibly with devices down to 5 nm lateral dimensions, the lifetime of a 'node' will likely be very protracted as the maximum benefit is derived from a particular set of device dimensions. Scaling is becoming primarily driven by density improvement, enabling parallel computing in multi-core processors, rather than by increasing absolute clock speed because without aggressively lowering the power consumption, the clock frequency of processors will be limited to about 4 GHz constrained by cooling limits. Technology boosters, optimisation and genuine innovation will likely keep a node lifetime going for up to a decade and it is essential and highly appropriate that European academe contributes to these developments. Power reduction, minimized leakage and faster heat dissipation will be vital for higher clock speeds to be realised. In the much longer timeframe, other technologies could be suggested, but we suspect any serious candidate will still be a three terminal field-effect device with similar issues of access resistance, leakage, silicon real estate area and fabrication complexity which will all be informed by work directed to highly scaled CMOS.
Continuing development and refinement of the technology will sustain and require very important research for decades to come, much of which would be appropriately based in academe. Such research will involve innovation and new insights covering the whole matrix of performance levers, for example channel engineering encompassing new materials such as Ge, III-V materials, C;, strain, wafer orientation, device architectures – including 1D and 0D structures, integration in the third dimension, embedded memory, ever-improving contacts and gate stacks; all backed up by effective modelling with increasing emphasis on predictive simulation at both device and system level.

Whilst 22 nm technology seems realistic with immersion lithography and double exposure, EUV (severely delayed and expensive) or imprint lithography are required for smaller feature sizes.
The adoption of Silicon-on-Insulator (SOI) substrates for the manufacturing of mainstream semiconductor products such as microprocessors, has given SOI research an unprecedented impetus. In the past, novel transistor structures proposed by SOI scientists were often considered exotic, costly or impractical, but the recent success of SOI in the field of microprocessor manufacturing has finally given this technology the credibility and respect it deserves.
The classical CMOS structure is reaching its scaling limits and "end-of-roadmap" alternative devices are being investigated. Amongst the different types of SOI devices proposed, one clearly stands out: the multigate field-effect transistor (multigate FET). The planar and vertical (FinFET-like) double-gate transistors enable better electrostatic control of the channel(s), hence a more aggressive scalability, reduced leakage currents, and enriched functionality. Each separate gate can play different roles (for memory, mixed signal processing, etc.). The challenge is for designers to unveil innovative circuit architectures for the benefit of reducing the transistor count and enhance the performance. The nanowire device has a general "wire-like" shape with a gate electrode that controls the flow of current between source and drain along the various surfaces of the wire. Multigate FETs are commonly referred to as "multi(ple)-gate transistors", "wrapped-gate transistors", "double-gate transistors", "FinFETs", "tri(ple)-gate transistors", "Gate-all-Around transistors", etc. The

International Technology Roadmap for Semiconductors (ITRS) recognizes the importance of these devices and calls them "Advanced non-classical CMOS devices".

Channel Materials:
Strain and quantization effects are the key enablers to optimize the channel materials for ultrashort MOS devices. Aside from channel mobility, injection velocity, access resistance and electrostatic control at nano-dimensions become more and more crucial. Strain platforms and strain transfer methods are needed to further boost mobilities and to lower power consumption. High Ge content SiGe and Ge on insulator platforms (of high quality) should be established. This will also enable the integration of III/V semiconductors on silicon, for n-channel devices and, in particular, for new functionalities, such as RF applications and optoelectronics.
Alternatives to (100) oriented substrates will gain relevance. Si(110) seems to be attractive due to higher hole mobilities and the possibility of realizing uniaxially strained layers at a wafer level. Because of severe growth issues, only limited data are available as yet. Also Ge(110) has barely started to be investigated and other orientations remain purely academic.
Selective epitaxial growth in narrow windows of highly lattice mismatched semiconductors will gain interest to improve the crystal quality and to grow nanodots or –wires.
The use of heterostructures in MOSFETs in combination with high(er)-k gate stacks is at its very beginning of exploitation.

Access Resistance:
One of the key limitations of nanodevices is the access resistance. While NiSi has become the most used silicide, further reduction of the contact resistance is needed. In addition, layer and line edge roughness should be reduced to minimize variability. The latter is most crucial for Schottky barrier transistors. Epitaxial contacts and new alloys have to be investigated. Nanowire metallization is still in its infancy.

Gate Stacks:
Considering the requirements given by ITRS for LSTP ”multigate SOI”, there is a doubt whether the silicon film thickness below about 4.5 nm will be possible. The present standpoint in the literature seems to be that interface scattering is expected to kill the mobility for thicknesses below this value. On the other hand, for the required values of oxide thickness, the ratio between physical gate length, L_{LSTP}, and channel potential decay, seems rather conservative. Whatever guess is best and assuming the validity of the ITRS forecast, it should be possible to find gate insulators with the fundamental property $k \times \Delta E$ to fulfill the leakage requirements. The reason is that the leakage data are very relaxed, from 190 to 390 mA/cm^2. The problems will be to find metal oxides/silicates which (i) are chemically stable with Si and (ii) structurally stable up to about 700 C, (iii) have low enough interface state densities and, which might be the hardest problem, (iv) have controllable bulk trap properties. Ternary compounds will be necessary. As the efforts to refine the properties of HfSiO probably will be intense, this material may be possible for use even at the 22 nm node. In ITRS-terms, this means in about 5 years. Beyond 2016, a new material with a higher $k \times \Delta E$ product, in the range 45 - 50, must certainly be found. A number of alternatives exist like LaLuO ($k \times \Delta E$ = 60 eV) or GdSiO ($k \times \Delta E$ = 48 eV). If the demands (i) – (iv) above can be satisfied, these materials might be possible for use down to the 14 nm node, which offers a 10 year perspective.

Beyond the 14 nm node, when the gate length comes close to about 5 nm, the transistor function becomes considerably modified. A 5 x 5 x 3 nm^3 piece of silicon on SiO_2 is a quantum dot even at room temperature. This will change the silicon CMOS paradigm and new geometries will be needed, possibly still to a large part based on silicon technology, but with a more clear use of quantum mechanical effects.

Opportunities for FETs and Memories:
The nanowire (NW) structure allows scaling to move beyond the boundaries imposed by classical transistor architectures, leading to the definition of novel types of FET device for future nanoelectronics applications such as junction-less transistors (where processing thermal budget is no longer a manufacturing bottleneck), 4-independent-gate transistors, etc., single electron memories where a Si dot is self-aligned to a Si nanowire to address this extremely tiny memory cell, and tunneling transistors that can switch with subthreshold slopes below 60 mV/decade, a theoretical limit that cannot be overcome by any classical transistor structure. This slope sets a practical limit to the reduction of supply voltage, and, therefore, of power consumption of a circuit. The double-gate MOSFETs are suited for innovative schemes of capacitor-less DRAM, utilizing the floating body of SOI devices. The magic opportunity and goal is to conceive a 'universal' memory which can combine volatile and non-volatile functions depending on the application. The market opportunity, offered by the replacement of classical memories, is huge.
Thanks to the huge increase of its surface-to-volume ratio, the Si nanowire electrical behavior is quite sensitive to its surrounding environment and thus it constitutes an ideal elementary block for highly sensitive biosensors.

Challenges:
In order to bridge the gap between the theoretical concepts and the design of circuits for applications, research laboratories in universities must focus on several fundamental issues. Please see below an exhaustive list of subjects on which we should concentrate.
- Multi-channel MOS: stacking of channel - issue related to the definition of the gate electrodes (self-alignment) - gate first process? Gate-All-Around MOS;
- Multi-gate (MG) architecture for MOS: reduction of the fringing capacitances (connection) between gate electrodes and S/D contacts for improving their dynamic behavior (RF performance);
- Use of independent multiple gates to achieve circuits with enhanced (or revolutionary) functionality and compact real estate. For example, use of double gates for advanced memories: capacitorless DRAM, multi-bit nonvolatile memories, universal memory combining volatile and non-volatile functions;
- Deeper analysis and exploitation of the potential offered by Ultra Thin Body Thin BOX (UTB) for closing the gap between Single and Double Gate SOI MOSFETs;
- Integration of nano-objects by combining the top-down and bottom-up approaches (contacts and interconnections defined by classical top-down approach and grown of Si NWs);
- Source / drain engineering: Schottky contacts (low temperature process) for reducing the contact resistances and overlap capacitances, issues related to the roughness of the silicides for ultra short devices;
- Oxidation rate and etching selectivity between Si and Ge for defining self-alignment nano-objects (for instance, Single Electron Memories);
- Issues related to the nanocharacterization of Si NWs (physical - roughness, dimensions, ... and electrical characterization - surface states, transport, contacts, high input impedance, ...). How can we characterize nano-volumes containing one impurity or one defect and only 1000 Si atoms?;

- Conceive characterization methods able to discriminate the properties of each channel, oxide or interface in MG FETs;
- Strain engineering for Si NWs: process induced versus strained substrate solutions, to boost the carrier mobility and lower power consumption;
- Select more adequate semiconductors and buried insulators able to outperform the classical marriage Si-SiO_2. For example, the co-integration of Si with Ge or III-V compounds offers enhanced mobility and speed and the use of high resistivity silicon substrate combined with a trap-rich layer vanishes the conductive coupling into the substrate which is a critical issue for SoC. High thermal conductivity buried dielectrics will solve the critical problem of device self-heating. They can also offer embedded strain and memory capabilities. One should also think about combining electronic and optical functionalities in a single chip;
- Take better advantages of the high aspect ratio (surface/volume) of Si NWs for sensing applications: biosensors, giant piezo-resistance effect (gauge sensors),
- When examining innovative small volume devices, new physical mechanisms are likely to be discovered. It is essential to explore their practical applications. For example, the super coupling effect prohibits the coexistence of accumulation and inversion layers in the same body, a typical situation used in capacitorless memories;
- Variability issues (matching) of Si NWs and thus the impact on basic circuit blocks. We must bridge the gap between technology and design. To do so, we must now start working on basic designs, for and using the long term process/device concepts. This is particularly true when thinking about small slope FETs, tunnel FETs, nanowires, We have to keep in mind that one technology node may last only for 2 years whereas one new design methodology is introduced only every 7 years.

3. Ultra low power era: small slope devices and low power design

The race for Ultra Low Power is becoming a prerequisite to allow the scaling of the device dimensions below 22nm and down at least to 11nm node, primarily driven by density improvement which in turn enables parallel computing in multi-core processors. Without aggressively lowering the power consumption the clock frequency of processors will be limited to about 4 GHz because of reaching the cooling limits.

In the search of a truly competitive small-slope switch:

In past decades, the focus of the semiconductor industry has been on scaling to improve performance in terms of speed (CV/I) and reduction of die area, and hence reduced cost per operation. This has been an extremely successful approach, but as devices are scaled much below 100nm, new challenges appear. Most notably, the transistors become leakier resulting in a larger off-current. The rise in leakage current in combination with an increasing complexity and interconnectivity of today's computer chips means that the power consumption increases dramatically, and eventually the standby power consumption might even exceed the dynamic power actually used for computations.

Therefore, the semiconductor community is looking for new devices and architectures which are expected to bring added value to CMOS by presenting an abrupt subthreshold slope (S), better than the 60mV/decade at room temperature found for ideal conventional MOSFETs. This approach can provide extremely low Vdd operation together with acceptable Ion/Ioff ratio and therefore small off-currents and ultimately small standby power.

A small slope switch must feature a value of S smaller than 60mV/dec at room temperature, which is the limit for a conventional MOSFET due to the below-threshold source-drain diffusion. Therefore, the smaller the value of S, the faster the transition from the on- to the off-state and vice versa. A low S will permit lowering of the supply voltage to below the ~0.5 V limit of standard CMOS while retaining an acceptably low Ioff, leading to savings in both stand-by and dynamic power and hence extending the CMOS roadmap by several generations. Today, there are many candidates in the quest for the ideal small-slope switch but the requirements of room-temperature operation and CMOS compatibility rule out most of them.

Tunnel FET:

From this realistic point of view, the most promising small-slope switch today is the tunnel FET (TFET), where the drain current flows by source-drain inter-band tunnelling modulated by the gate voltage. While retaining full CMOS compatibility, including the source-drain-gate three-terminal layout, the TFET is not limited to S > 60 mV/dec and permits a variety of possible implementations, including the exploitation of new device geometries and materials. In the past 6-8 years, several TFETs were proposed including some from Europe and although much work is still needed both theoretically and experimentally, the stage seems set for the realization of truly competitive switches, exploiting new concepts, based on local hetero-structures of small band gap semiconductors, and promising low power consumption and also high switching speed. Recently, multi-gate devices (double-gate, FinFETs) have been proposed for boosting the performance of tunnelling FETs (smaller swing down to 2mV/dec, higher Ion, etc.). Also graphene-based channels have shown extremely interesting potential for TFET operation, thanks to their low band-gap (in the few hundreds of meV range) low effective mass, and low quantum capacitance, enabling high Ion and an Ion/Ioff ratios in the range of 10^4 even with a supply voltage lower than 0.2 V.

Finally, new emerging concepts are gaining attention in the search of a better, CMOS compatible switch. One example is the Junction-less transistors where the presence of one doping type in the S/D and channel regions prevents the needs of drastic doping gradients with widths of a few nanometres, while the confined electrostatics of the UT-SOI allows for good Ion/Ioff ratio.

Ferroelectric materials:
In the race for ULP, an interest subject is the integration of ferroelectric materials which have applications in memory, sensors and actuators, high permittivity voltage controlled capacitance and possibly small slope switches. Theoretical and experimental work is needed to understand many physical aspects including apparent "dead layers" at interfaces and possible effective negative capacitance which may be used to reduce subthreshold slope.

Circuit and system architectures:
Apart from improving the switch sub-threshold slope, the main issue in the low power design is device variability. In order to cope with the increasing impact of variability, the following topics should be thoroughly considered and investigated:
(i) Design of devices with low variability using low doped channels.
(ii) Predictive physical modelling of variability that supports such devices design.
(iii) Statistical compact models that include the variability and can allow statistical approach to low power design.
(iv) Innovative design strategies that are robust and variability-resistant including redundancy, error monitoring, self healing, self organisation etc.

Up to now, ultra-low-power sub-/near-threshold CMOS logic design has been restricted to low-performance applications (RFID, biomedical, sensor networks) due to high delay penalty. However, CMOS technology scaling will broaden the potential application spectrum to mid-performance applications in the "mainstream-silicon" low-power market.
The operation at subthreshold Vdd (0.3-0.5V) under moderate (1-100 MHz) timing constraints leverages MOSFET design paradigms that significantly differ from existing ITRS HP/LOP/LSTP roadmaps. Indeed, the main focus is a much tighter control of short-channel effects (subthreshold swing and DIBL) and of variability, as their impact is magnified in subthreshold regime. To achieve these targets, some device constraints related to high-performance nominal-Vdd operation are significantly relaxed such as series resistance, mobility and gate/junction leakages. Additionally, circuit design techniques for reliable subthreshold circuits such as design-level Vt selection and run-time adaptive body biasing yield extra targets for MOSFET design and technology development.
This can lead to subthreshold-optimized dedicated CMOS processes at 32/22nm nodes, whose R&D costs would be supported by the access of sub-threshold circuits to mainstream-silicon markets.
Amongst the potential technologies for developing such a CMOS process, ultra-thin-body fully depleted (FD) and accumulation mode (AM) SOI, multiple gate architectures or small swing devices appear as efficient and realistic candidates, provided that 1) multi-Vt devices are available with 2) adequate back-gate coefficient and 3) sufficient SRAM stability. The latter might favour new memory cell architectures such as 7-12T SRAM cells now under consideration.
Finally the development of new device architectures for ultra-low power circuits should be supported by a device-circuit co-design, in order to test the potential of new devices with respect to standard MOSFETs by using appropriate vehicle circuits. This includes the need for adequate compact modelling incorporating the usual process-voltage-temperature variations

in a manner that is both complete, including cross-correlations in the variations on single parameters, and efficient to allow for high-speed circuit simulations, including Monte-Carlo analyses made difficult in subthreshold since distributions become log-normal instead of Gaussian, as well as dynamic effects and noise.

4. Adding functionality to CMOS

The topic covers long-term research challenges in the so-called “More than More” domain which exploits the fact that improved performance does not come solely from scaling but also from increasing system functionalities.

Integration of technologies and materials: placing all together

MEMS/NEMS and bio-sensors: these indeed require well-controlled interfaces (at nano scale), excellent electrical parameters such as coupling factor (i.e. high permittivity), good barrier (low leakage).

Tunable RF- and mm-wave circuits: continue efforts on MEMS and NEMS, matching automation (e.g. impedance adapters).

Development of mm-wave circuits (60 GHz - 90 GHz range): passive components (wave guides, filters, power splitters). Here the challenge is to improve the quality factor of integrated transmission lines in order to achieve low-loss miniaturized transmission lines.

Integration of low RF loss dielectric microplates on Si to provide a local substrate for RF integration (high Q inductors in CMOS processing) is very challenging. A promising approach in this respect is porous Si RF microplate technology.

Wireless interconnections intra- and inter-chip: integrated antenna design taking into account technological impact like dummies and EMC.

Integrated or embedded passive components in Si, featuring high-precision (<1% tolerance), low TCR, large value/high density (3D structures) for energy harvesting applications.

Integration of ionic and electronic interfaces and devices for single molecule detection (surface functionalization by physisorption and chemisorption processes, self assembling monolayers, soft lithography of biomolecules).

Integration of nanostructures in electronic substrates (nanopores, nanogaps, nanorods, nanotubes, nanowires, nanopillars, nanocrystals, graphene and carbon nanotubes structures).

Smart packaging of electronic systems (flexible substrates, smart fabrics, chip-to-MEMs structures, flexible packaging, microbattery integration, microfuel cells, mixed plastic-silicon electronics).

New architectures for advanced targets: going into the small

Systems that can work for extended periods of time (> 1year) without external power supply:

Requirements: i) ultra low power systems; ii) integration of power miniaturized supply systems; iii) intelligent architectures for wake-up systems, time synchronizations and power management.

Systems that can sense in the small: ultra miniaturized sensor for ubiquitous applications:

Requirements: i) devices and architectures for ultra-small cameras; ii) device, architectures and packaging for data acquisition and storing in ultra-small environments.

Systems for short range (< 1m) communication and localization:

Requirements: i) highly reliable short-range communication; ii) accurate short-range localization by UWB or other techniques.

Specific applications
In-vivo biosensors (lab-on-a-pill, implantable devices, neuro-prostheses for rehabilitation devices, sentinels)
Advanced instruments for diagnostics and theranostics (silicon-based lab-on-a-chips, POC devices)
Completely autonomous monitors for environment, buildings, automotives.

Merging nanoelectronics and photonics
Integration of fast optoelectronic circuits in a cost-effective nano-electronic fabrication process is an important aspect for the realization of future communication systems. Some important innovations during recent years have enabled silicon-based opto-electronic technology. Several photonic elements are already in quite an advanced stage of development but modulators and particularly a low power light source still require much work. Merging of electronic and photonic technologies is urgently required as communication bottlenecks between and within chips are increasingly prevalent.
The anticipated long term research objectives in this area that should be addressed by the silicon nanoelectronics community are the following:

1. Integration of optoelectronic functionality in a nano-electronic fabrication process. Key process steps such as patterning of waveguides with low optical loss/surface roughness, tolerances and wavelength of resonance structures by well controlled line width and spacing, use of non-conventional oxides (grown by ALD/PLD) for index contrast with potential electrical tuning. The use of electrochemistry for the fabrication of 2-D or 3-D photonic devices on Si is one of the challenging issues.
2. Layout and design considerations for an approach with standard cells for the optoelectronics functionality in analogy with standard layout of cells and design rules for the electronic part of the chip. Monolithic integration of the electronics and optoelectronic components is the ultimate goal for mass producing consumer applications. Serious consideration of how to optimize layout and interconnects for the very small and dense electronic components around the generally large photonic components is required.
3. Basic research on the optical properties of strained silicon and silicon-germanium and their future applications. In particular, nano-silicon process technology to explore modulator designs for silicon based opto-electronic transceivers.
4. Heterogeneous integration of group III/V materials, to utilize their suitable opto-electronic properties, directly interfaced with highly scaled CMOS circuitry.
5. The interface between electronic and optical part of the chip requires sophisticated high speed driver circuits. The design of such circuits should be given emphasis even in the context of a hybrid solution where the optical part is done in traditional III/V materials with a silicon driver circuit attached by bonding.

Other long term challenges
There are several opportunities to apply nanoelectronics and associated fabrication techniques to move into new territories to further extend its range and depth of influence on our society. These can only be loosely defined at the moment but would involve the development of new technologies or even disciplines including:

Soltronics
This concerns using nanofab-nanoelectronic techniques to help society live by /or live with our sun's radiation. This could include developments ranging from enhancing the efficiency of

silicon-based solar cells, testing the potential of nanostructures for photovoltaic applications, right up to controlling climate change.

Flexible electronics

Recent research results have shown that silicon can successfully compete with organic technology in the area of flexible electronics. The low mobility and instabilities of organic transistors constitute a limitation difficult to overcome for organic processes. Very recently it has been demonstrated that SOI CMOS devices fabricated on a silicon wafer can be transferred to plastic substrates. It has also been shown that silicon electronics can even be printed by Ink Jet printers. Silicon-based flexible electronics appears as a very promising field of research that can contribute to revolutionize the wearable and stretchable electronics industry.

Cooltronics

This involves using silicon based SiGe processing techniques to enable super cooling (< 50mK) of critical components on a chip to, for instance:

(i) give greatly increased sensitivity of radiation detectors (from x-ray to infra red) as needed for example to detect fluorescence from medical assays facilitating point of care diagnostics and much more in the medical field. Such sensitive light detection facilitated by the super-cooled components is claimed to be "the future of biology".

(ii) enable the realization of a viable quantum computing technology, which requires qbits operating at 20mK.

Silicon Laser

Silicon based lasers continue to the holy grail and studies are needed to advance this to a working reality. For instance, the Si-Ge quantum cascade laser which would have major applications in medical imaging and security. Integration of such structures in CMOS is a major challenge but such devices also have potential as the light source for silicon photonics, to help relieve inter- and intra-chip communication bottlenecks.

5. Templated self-assembly of functional nano-structured materials with CMOS compatibility

Semiconductor nano-structures with periodic and aperiodic features constitute key elements for future advanced ICT devices. Attractive enhancements in performance for the manipulation and transmission of information are expected if the quantum nature of nanostructures come into play. To integrate these nano-structures into the real CMOS environment, however, it is essential to fabricate them with a controlled size and period.

Templated self-assembly (TSA) methods combine top-down (lithography) and bottom-up (self-assembly) approaches for creating nano-wires, rods, and dots. By using physical templates to alter the surface environment, self-forming and self-ordering processes can be initiated in materials systems that have limited or no inherent order.

In this context two major methods for a templated self-assembly can be pursued in the future: Deposition methods including atomic layer epitaxy (liquid-phase, vapour phase, molecular beam, hetero-epitaxy) as well as advanced ion erosion techniques that open the way for the fabrication of self-ordered and aligned nanopatterns within a CMOS environment. CMOS compatible deposition routes include self-organized growth of vertical nano-wires by Chemical Vapor Deposition, periodic selective epitaxy on nanoscale and formation of highly precise nano-structures through truncated de-wetting.

For the ion erosion approach, low energy ions are accelerated onto a semiconductor surface. The interplay between enhanced surface atom mobility and angular dependence of the sputter yield leads to the formation of periodic hexagonal dots and line patterns, respectively. By introducing templates, i.e. lithographically predefined, etched mesa-topologies and/or dislocation templates, it is expected that the spatial phase information of the templates is mapped down to the resulting dot pattern and thus that a long range spatial phase coherence over large areas might be achieved.

Concerning the fabrication of nanowires and nanodots by self-assembling CVD technology, integration is still challenging. The control of the position, the size and the doping has to be achieved by using CMOS compatible technology. Another key feature in such high ratio S/V is the passivation of the surface states which influences strongly the electronic properties. Finally, contact issue should be addressed and compared with the standard value obtained by the top-down approach.

Still challenging key problems remain kT-induced variations of size and periods associated with inherent thermal fluctuations. Future efforts have been focused to narrow the distribution in size and period of self-aligned nano-structures to gain the real advantage of quantum phenomena for ICT.

The main field of application for all TSA-techniques discussed, remains the aim for achieving the highest density for data storage. Cost effective process technologies for highly periodic feature size dot patterns will open the door to multi-Tb/sq. inch data density.
Regarding the convergence of electronic nanotechnology and photonic information technology, the use of sub-wavelength highly periodic surface topologies gives access to new photonic devices. For the fabrication of such structures on Si, electrochemical techniques, in combination with self-assembled masking layers directly grown on the Si substrate, offer a large potential for the local formation on Si of highly ordered 2-D or 3-D nanostructures.

Such masking layers are for example porous anodic alumina thin films on Si. Macroporous Si structures with straight pores of diameter in the range of few tens of nm up to few hundreds of nm might be fabricated after pre-patterning through such masking layers and used in photonic device design and fabrication.

6. Carbon Electronics integrated on CMOS platform

A large body of fundamental research on carbon electronics can be reviewed today as dominated by the mother of all graphitic structures: Graphene, a flat monolayer of carbon atoms packed into a 2D honeycomb lattice, appears to be the building block of all graphitic materials considered up to now (fullerenes, carbon nanotubes, 3D graphite).

Today graphene, or 2D graphite, attracts considerable attention, not only by the physical science community but also at an astonishing rate by leading laboratories in the ICT industry. All the progress reported from the physical science community reveals great potential for nanoelectronics, including memory, logic, analog, and optoelectronic devices. In addition attractive possibilities appear on the horizon of highly connected and sensitive sensor systems. For future ICT development, silicon based technologies will approach their fundamental limits and new alternatives with exceptional potential are urgently required. The potential of graphene for electronics is based mainly on the high mobility of its charge carriers and the fact that the mobility remains high even under extremely high electric field induced carrier concentrations. It seems feasible to retain such a high mobility also in the presence of chemical doping, indicating the possibility of ballistic transport on a sub-µm scale at 300 K. Thus the first entry point for graphene electronics will definitely be for application to high frequency components where the inherent advantage of high mobility is of paramount importance.

The integration of graphene into a CMOS platform, however, depends critically on the availability of high quality and uniform graphene films on CMOS compatible substrates. Up to now, large area synthesis of high quality graphene films on SiC wafers and metal substrates have been published. Two recent papers also report the fabrication epitaxial graphene on SiC with an intrinsic gap of 0.26 eV induced by spontaneous break of symmetry in the graphene structure. The transfer onto CMOS compatible substrates has been demonstrated in principle, but it does not seem to be feasible for large scale production. For mainstream logic applications, the metallic character of intrinsic graphene poses a major problem. Through constrictions or chemical doping, a transition into a semiconducting state can be facilitated. It is expected that for GNR, graphene nanoribbons, with a width of less than 3 nanometers, high Ion/Ioff ratios can be achieved that opens the way to a digital graphene transistor world. However, GNRs pose two additional issues: on the one hand, they require single-atom precision in the lateral lithography, since the bandgap is strongly oscillating as a function of the number of dimers in the transverse direction; on the other hand phonon scattering and edge roughness may reduce mobility in very narrow GNRs down to values typical of more common semiconductor materials.
One other clear issue that needs to be solved is how to provide a good insulating layer in combination with graphene, which does not result in a reduction in the device mobility. Without solving this problem the advantages of graphene are quickly lost.
Far more attractive and rather revolutionary, is a route to all graphene based electronics, whereby graphene acts as a highly conductive medium in which selective semiconductor behavior is introduced on a nanoscale either by chemical doping or by nano-structuring. This route opens the way to a new path of switching structures beyond the current silicon CMOS concepts. However at the moment, it is not clear that doping will not greatly limit the mobility. Particularly the convergence of Coulomb blockade processes and molecular electronics offers great potential as these structures could still be fabricated with the top-down approaches currently available in the silicon world. The big advantage of this revolutionary approach is that all these components with different ICT functionalities, including channels,

barriers or interconnects, could be carved out from the same graphene sheet by means of electron beam lithography and dry etching. With that, ICT systems at the nanoscale may be truly achievable.

The efforts in the ICT community should be focused on the following immediate challenges:

1. Large-area synthesis of high quality and uniform graphene films on CMOS compatible substrates, suitable for top down fabrication schemes.

2. Controlled changes of transition into semiconducting states in graphene sheets by selective bandgap engineering via chemical doping or lateral constrictions, including passivation of the doping layer.

3. Realization of valuable demonstrators for high speed applications (THz), FET-SET combinations and ultra sensitive intelligent sensor systems approaching the biomedical ICT branches.

4. Development of characterization techniques for assessment of the quality and optimization of fabrication process.

7. Characterisation at the nanoscale

The scaling down of feature sizes in modern CMOS processes imposes very rigorous requirements for characterisation methods with respect to accuracy and reproducibility. To cope with the challenges of sub 22nm nodes, the currently established measurement techniques must be further improved or substituted by novel innovative approaches. The challenges for characterization of nanostructures could concern the physico-chemical analysis, the electrical property measurements as well as the reliability or instability issues.

For the characterisation of one-dimensional doping profiles, High-Resolution Secondary Ion Mass Spectroscopy (SIMS) is the most commonly used technique. A major parameter to be controlled is the surface roughness induced by the primary beam, being the origin for the degradation of the depth resolution. Complementary to SIMS, electrical profiling methods such as Spreading Resistance can be used. An increasingly severe problem for electrical profiling is the difficulty of interpreting spreading-resistance measurements in terms of actual carrier concentrations. This could be complemented by differential Hall effect measurements but with increased spatial resolution.
In the case of two-dimensional dopant imaging, Scanning Capacitance Microscopy (SCM) and Scanning Spreading Resistance Microscopy (SSRM) are the most widely used characterisation techniques. SCM stills lacks spatial resolution and reproducibility compared to SSRM. The enhancement of the SCM method requires a better control of the oxide layer, a better control of the preparation of the samples for an enhanced resolution (bevels), an enhancement of signal to noise ratio, and a strong knowledge of the physical mechanisms involved in the imaging process. For SSRM, the upcoming challenge is to extend its capabilities to 3D shaped devices.
The materials and processes necessary in 22nm and beyond CMOS processes require improved characterisation of the composition and material density at the interfaces of high-k dielectric/metal and high-k dielectric/Si. For this purpose, depth profiling techniques like SIMS, Medium Energy Ion scattering (MEIS), AES and XPS need to be improved, e.g. by enhancing sensitivity or by model-based interpretation of the depth profiles. STEM-EELS coupled with HR-STEM analyses could be improved to determine the chemical element profiles at nm scale. New methods for interpretation of XPS and ATR-FTIR spectra, Spectro-ellipsometry for better understanding of chemical bonding should also be developed.
Apart from these techniques, X-ray based techniques such as XRR and XRD permit to extract relevant material properties such as crystal structure, texture, grain size, density, film thickness etc. While for the analysis of thicker films or large surface areas, normal X-ray systems are well suited, one has to turn to much brighter X-ray sources (Synchrotron radiation) when analysis is needed within the nanoscale device structures themselves or on very thin films, thus, when count-rates become insufficiently low.
Advanced devices will be more and more sensitive to the various mechanical stresses induced by the manufacturing process steps. These stresses can be beneficial to improve the CMOS performances by increasing the carrier mobility in the channel but can also be detrimental by increasing the stress-migration and electro-migration probabilities and so reducing the reliability of interconnects. Techniques such as SEM-EBSD, TEM-CBED, dark field holography, Raman spectroscopy, X-ray or MEIS , 2^{nd} harmonic SE should be improved to enhance the strain measurement resolution at the nanoscale. Tip-enhanced Raman spectroscopy (TERS) has the potential to *non-destructively* probe both strain and material composition with lateral spatial resolution <10 nm and significantly better vertically. Suitable

tip development and new theoretical models of the enhancement effect for new materials are required. Nm-scale strain analysis of 3D devices such as nanowires requires development of non-contact mode TERS techniques and advanced optics.

To date the electrical characterisation of advanced CMOS devices featuring short channel length and ultra thin gate oxides presents major difficulties. This is mainly due to gate length or gate width shortening, which renders effective channel length/width extraction problematic. Moreover, huge gate leakage makes it very difficult to obtain reliable measurements of C-V characteristics, which in turn, prevents the correct extraction of the basic parameters of MOS structures. Therefore, new methodologies, for extraction of MOS parameters have to be worked out for sub 22nm CMOS generations. The main challenges should concern the dielectric-channel interface characterization, which becomes more important in nanostructures like nanowire with increased surface-to-volume aspect ratio, the assessment of transport mechanisms in ultra-short devices where ballistic effects are likely to occur, and, reliability or instability issues related to few carrier number phenomena.

The characterization techniques generally used for interface quality evaluation such as capacitance-conductance measurements, charge pumping, generally fail to work as the device surface is scaled down or the gate dielectric is too leaky. This implies revisiting their resolution and operating principles to be applicable to small dimension devices or to be used with appropriate test structures. In this respect, one major problem still remains for EOT extraction in the case of ultra-thin dielectric layers, which could be overcome by using high frequency capacitance measurements. For interface defect density evaluation at very small device area, alternative techniques based on channel current measurements could advantageously be employed, such as current-DLTS, LF noise spectroscopy or dynamic transconductance since they are not area dependent. All these techniques should also be adapted to novel architectures such as FD-SOI, multi-gate devices or nanowires where several interfaces could play a role.
The electrical characterization should also be performed in a wide frequency range (up to RF) in order to reveal the device limitation at actual operating frequencies. A number of effects manifest only (or disappear) at high-frequencies and, hence, need investigation over a wide-frequency range. Moreover, with device downsizing, extrinsic device parameters (or parasitics) become very important. It can be imagined that even in the limit, the ‘extrinsic’ device dominates the ‘intrinsic’ one. Here, RF characterization is almost the only tool to address separately intrinsic and extrinsic parameters and properties. Intrinsic capacitance characterization and modelling is also given little attention at present. The wideband characterization is of interest for developing wideband models for designers but also to give useful technological information about the fabrication options to technologists. It is worth emphasizing as well, the importance of including special test structures, such as for example, p-i-n and RF devices at the very beginning of technology development and assessment, particularly for the first mask set, given their very high cost..

Another critical issue is the assessment of transport properties, which ultimately control the final performance of devices. More specifically, critical analysis of low field transport (mobility) has to be performed for ultra short devices, e.g. with novel dielectrics, in order to establish clearly the impact of new channel and gate architectures on device performance. The challenge is to measure accurately the carrier mobility in small size devices using or adapting the well-known split C-V technique to small area devices, or adopt more appropriate methods based on the geometric magnetoresistance technique, which avoids the need for effective channel Leff determination. The latter is a key issue for ultra-short transistor where Leff

assessment is very critical and cannot be performed with conventional MOSFET parameter extraction methodologies. This would require development of new Leff extraction techniques based on capacitance or other type of measurements at low or high frequency. In this context of scaled devices, the increasing role of parasitic source-drain or gate series/access resistances is also a major concern, since they could limit the device performance in DC or RF operation. This topic should also be addressed carefully for the precise assessment of the extrinsic parasitic element of nanostructures.

Another hot topic in this context is related to the reliability and stability of new devices. Generally, these issues are not addressed at early stage of device development but it might be useful to determine the architecture or material best choices based on reliability criterion in the perspective of applications. This would allow discrimination of weak points in new device architectures with respect to possible environmental operating conditions: high temperature, low temperature, high voltage, radiation etc. New scaled devices will also suffer from reliability and variability issues related to their nature involving few-electron phenomena. This could imply huge sensitivity to SEU, radiation or information retention problems.

8. Challenges in simulation

As we all know there is nothing on the 20 years horizon that could replace the CMOS technology that underpins every aspect of life. Independently of the decisions of the European semiconductor companies we need to keep in Europe strong knowledge in advanced CMOS technology and devices starting from the academic establishment. Without such knowledge, in a relatively short time, not only the development of future technologies but the design of the future chips and integrated systems will become impossible in Europe.
Due to the increasing complexity of future advanced CMOS technologies, including new materials, new processes, and new architectures, multi-physics and multi-scale (hierarchical) modelling methodologies will be extremely relevant and necessary.
The possible exploitation of new channel materials as well as the optimization of the strain engineering are topics that range from the description of the band-structure to the development of compact model, by going through the physically based Technology Computer Aided Design (TCAD) device modelling.
The understanding and engineering of the material properties in nitride based (TANOS) and innovative (i.e. resistive, ferroelectric) non-volatile memories is another topic that goes from the atomistic simulation of the trapping properties of the nitride sites to the conventional engineering models for the program/erase simulation and for the device optimization, up again to the compact model area.

Most relevant topics in this “More Moore” scenario are the following:

First principle (interface, size and shape effects on band structure)

Quantum transport based on Tight Binding with parameters extracted from the first principle simulations

Multisubband MC in realistic 3D geometries with ab initio scattering from dopants, interface roughness, body thickness fluctuation

Direct, deterministic solver of the Boltzmann equation keeping the full-band structure and the exact scattering rates

MC calibrated hydrodynamic drift diffusion transports

Compact models including quantum and atomic scale effects

Verification of TCAD model via well calibrated experiments

Verification of compact models via calibrated TCAD modelling results and experiments

Efforts to bring the accuracy of hole modelling at the same level of electrons

Efforts to account for mechanical strain at each level of device simulation, for both electrons and holes, and including non homogeneous and complicated strain fields.

New implementation of band-to-band tunnelling mechanisms for simulation of "steep-slope" devices exploiting strain, new materials, hetero-junctions, and unconventional geometries.

Problems: phonon-assistance, real band structure, pre-exponential factor, inhomogeneous fields, convergence for high values of the rate

New algorithms addressing the computational bottleneck of solving advanced device models should get some focus as well

Process modelling is an important area where an increasing gap needs to be filled by working on emerging problems like: DFT / MD / continuum modelling of thermal processing including the effects of defects, dopants and interfaces. Mechanical strain should also be considered, both for its effects and as a result of some process steps (for instance oxidation both creates strain and is influenced by strain). In the case of CMOS this is already an active topic for Si and SiGe but needs to be extended to new materials like Ge and GaAs, as well as gate stack materials. In the case of nanowire- and other new devices, similar materials / process modelling problems will need to be addressed.

The field of multi-physics and heterogeneous systems is of growing importance for Europe where a peculiar strength of the nanoelectronics industry is based on product diversification and specialization.

Here multi-physics simulation plays a fundamental role in the progress of integration of heterogeneous systems.

Besides, it should be mentioned that Europe holds a leading position in the TCAD and Electronic Design Automation (EDA) tools industry. Intensification of research in multi-scale modelling will contribute to strengthen Europe's leadership in this type of business, which is essential for the progress of nanoelectronics industry.

Areas of particular interest are the following:

- Device-to-device simulations
    - Photonics/electronics interface models for embedded optical microcavities, memories and fibre interfaces.
    - Ionics/Electronics interface models for biology applications. Modelling of functionalized surfaces, self-assembling monolayers, chemisorbtion and physisorbtion
    - Multi-scale modelling of nanostructures (nanopores, nanogaps, nanorods, nanotubes, nanowires, nanopillars, nanocrystals, graphene and carbon nanotubes structures) with electronic devices.
- Device-to-system simulations
    - Modelling of multi-scale packaging for flexible substrates and interconnections, smart fabrics, chip-to-MEMs structures, mixed plastic-silicon electronics systems.
    - Modelling of integrated energy sources such as microbatteries, microfuel cells, MEMS harvesters.
    - Compact modelling of nanodevices, in order to develop analytical device models suitable for their implementation in EDA design tools. Compact modelling of HV (high voltage) and analog structures.
    - Hierarchical modelling of noise in heterogeneous systems, particularly for systems to be used for detection of single/few molecules in Bio/ ICT systems.

- System optimization simulations
    - Modelling of RF MEMs systems, especially where interactions between mechanical modelling, thermal management and RF performance design should be optimized at device, package and system levels.
    - Technology-aware design for intra-die, inter-die and inter-wafer variations supported by suitable hierarchical models of variability covering different levels of abstraction.
    - Thermo electro-mechanical modelling and simulations comprising HDL and stress device modelling and simulations in varied environmental and aging conditions (soft errors, crosstalk, interference, EMC, robustness, reliability).