Substrate technologies for the on-chip integration of RF passive devices

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RF in Nanofunction

OBJECTIVES

To explore the potential of NWs and other nanostructured materials in on-chip RF applications

- To develop RF substrate technologies and novel RF passive devices

- To investigate the properties of NWs for their application in RF interconnects and nano-antennas
Outline

➡ Substrate technologies for RF passives – State of-the-art
➡ Nanostructured porous Si as a local RF substrate
➡ Comparison of RF substrates
➡ High performance RF passive devices on a local porous Si layer
➡ Conclusions
Towards the digital / RF analog SoC

The co-integration of high speed digital circuits with high performance RF analog devices increases chip functionality.

Advantages:
Better performance than multi-chip and system-in-package solutions (reduced size and power consumption, increased reliability, lower cost)

Power reduction is of major importance since:
1.3% of global electricity is today used to move bits!

Main bottleneck towards the digital/RF analog SoC:
The low resistivity CMOS Si substrate is not adequate for RF / mm waves

CMOS substrate
Resistivity: 1-10 $\Omega \cdot \text{cm}$
Dielectric constant: 11.9

• Substrate losses in RF propagation
• Device cross talk
Advanced Si-based substrates for RF passive integration

- **High resistivity Si (HR)**
  - **Drawbacks:**
    - High cost
    - Not compatible with the CMOS substrate
    - Parasitic surface conduction (coupling, non-linearity)

- **Silicon-on-Insulator on a high resistivity handle wafer (HR SOI)**
  - **Drawbacks:**
    - High cost
    - Parasitic surface conduction

- **Trap-rich HR SOI**
  - **Drawbacks:**
    - High cost

Commercialized by SOITEC
New name: eSI HR SOI
eSI = enhanced signal integrity

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Main requirements for an RF substrate

- High resistivity, low RF insertion loss
- Tunable effective permittivity at RF
  
  *Low dielectric constant for high characteristic impedance devices and low substrate noise (crosstalk)*

Solution within the SoC approach

A local substrate with reduced RF losses on the bulk low resistivity CMOS substrate
Material that meets the corresponding requirements:

Porous Si

A local porous Si substrate on the Si wafer
Main properties of porous Si

Porous Si can be fabricated locally on the Si wafer by electrochemistry

- Planar topography with the Si substrate is possible
- Compatible with conventional Si processing
- Thermal expansion coefficient similar to that of Si. As a result porous Si films as thick as several hundreds of μm can be fabricated locally on the Si substrate without facing cracking problems and mechanical failure
- Dielectric properties are adjustable by electrochemistry
Porous Si structure and morphology

A. Sponge-like porous Si layers on p-type crystalline Si

B. Porous Si layers with straight anisotropic vertical pores with diameter in the range of 30-50nm on p⁺ Si
Dielectric Permittivity of Porous Si

Porous Si relative permittivity $\varepsilon_{PSi}$ over the frequency range of interest:

$$
\varepsilon_{PSi} = \varepsilon_0 (\varepsilon'_{r,PSi} + j\varepsilon''_{r,PSi})
$$

where $\varepsilon_0$ is the vacuum permittivity, $\varepsilon'_{r,PSi}$ and $\varepsilon''_{r,PSi}$ are respectively the real and the imaginary part of PSi relative permittivity.

Parameters to be considered by an RF designer:

- $\varepsilon'_{r,PSi}$: variable due to Si nanostructuring
- **Loss tangent ($\tan\delta$)**: It incorporates both polarization and conduction losses

$$
\tan \delta = \frac{\varepsilon''}{\varepsilon'} + \sigma / \omega \varepsilon_0
$$
Porous Si dielectric parameter extraction

- We use Co-Planar Waveguides (CPW) on top of porous Si
- We measure their s-parameters using a VNA
- We compare measurements with their full-wave electromagnetic simulations using the HFSS (Ansoft Inc.) simulator
- We extract the parameters by choosing the best fit
CPWs on porous Si

Typical layout of CPWs on porous Si

Typical layout dimensions in μm
\{L, G, S, g\} = \{5000, 800, 90, 35\}

Dielectric Permittivity of Porous Si

\[ \varepsilon_{\text{eff}} \]

- \( S_{11} \) and \( S_{12} \) (dB)
- Frequency (GHz)

- Low loss tangent!

- Permittivity depends on c-Si resistivity

## Dependence on porosity

### $P = 70\%$

![Image a](image1.png)

### $P = 76\%$

![Image b](image2.png)

### $P = 84\%$

![Image c](image3.png)

### TABLE I.

<table>
<thead>
<tr>
<th>Porosity (%)</th>
<th>Simulation</th>
<th>Real part of permittivity – depends on porosity</th>
</tr>
</thead>
<tbody>
<tr>
<td>70</td>
<td>$\varepsilon_{r,PSi}$</td>
<td>3.79</td>
</tr>
<tr>
<td></td>
<td>$\tan\delta_{D,PSi}$</td>
<td>0.035</td>
</tr>
<tr>
<td>76</td>
<td>$\varepsilon_{r,PSi}$</td>
<td>2.79</td>
</tr>
<tr>
<td></td>
<td>$\tan\delta_{D,PSi}$</td>
<td>0.028</td>
</tr>
<tr>
<td>84</td>
<td>$\varepsilon_{r,PSi}$</td>
<td>2.33</td>
</tr>
<tr>
<td></td>
<td>$\tan\delta_{D,PSi}$</td>
<td>0.047</td>
</tr>
</tbody>
</table>

### Ref.

Effect of porous Si layer thickness

Measured $S$-parameters

Transmission \( |S_{21}| \)

Reflection \( |S_{11}| \)

1 \( \rightarrow \) $t = 150 \ \mu\text{m}$; 2 \( \rightarrow \) $t = 100 \ \mu\text{m}$;
3 \( \rightarrow \) $t = 50 \ \mu\text{m}$; 4 \( \rightarrow \) $t = 25 \ \mu\text{m}$;
5 \( \rightarrow \) $t = 10 \ \mu\text{m}$;

Measured normalized power loss of the 5 CPWs fabricated

Total system power loss: \( PL = 1 - |S_{11}|^2 - |S_{21}|^2 \)

Implementation of porous Si in standard CMOS

Theoretical design produced with full-wave Method-of-Moments simulations

<table>
<thead>
<tr>
<th>Layer</th>
<th>Metal 1</th>
<th>Metal 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pass2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pass1</td>
<td>M1</td>
<td>M2</td>
</tr>
<tr>
<td>IMD1</td>
<td>M1</td>
<td></td>
</tr>
<tr>
<td>ILD</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FOX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Porous Si</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Si</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Technology diagram for CMOS-compatible Porous-Si integration.

Dark Gray: Metal 2, Light Gray: Metal 1.
Comparison between different Si substrates

- Standard low resistivity Si (1-10Ω·cm) *(Std-Si)*
- High resistivity Si (>4KΩ·cm) *(HR-Si)*
- Trap-rich high resistivity Si *(TR-Si)*
- Porous Si (200μm-thick) *(PSi)* on bulk low resistivity Si

**Layout and dimensions of the CPW TL**

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CPW TLine on different substrates – RT characteristics (I)

Characteristics of a 2146μm CPW Tline on the investigated substrates.

\[ a = \frac{R}{2Z_c} + \frac{G}{2Z_c} \]

CPW TLine on different substrates – Harmonic distortion and crosstalk

Harmonic distortion at 900MHz of the 2146 µm long CPW TLine

Substrate crosstalk

The harmonic distortion for PSi and TR Si is negligible. The substrate crosstalk is reduced compared to std Si and HR Si (pure capacitive coupling)

Comparison of Si substrates – Effect of temperature on harmonics

(a) Characteristic impedance of the 2146μm TLine
(b) Effective relative permittivity of the 2146μm TLine

Effective resistivity of the 2146μm TLine

Harmonic distortion (2146μm TLine)
mm-wave CPWs on porous Si

CPWs on porous Si in the frequency range 1-110GHz

Two characteristic impedances: 50Ω and 140Ω

Measured (full lines) and simulated (dotted lines) characteristic impedance versus frequency.

(Resonances at 40 and 80 GHz are due to the specific TL length)

mm-wave CPWs on porous Si

Effective relative dielectric constant and phase velocity of the CPW TLines realized on porous Si

Attenuation constant of CPW TLs on porous Si

Very low attenuation constant, independent of the characteristic impedance, contrary to CPW TLs on a standard low-resistivity CMOS substrate

Good agreement between simulations and measurements

Accurate prediction for further realizations

mm-wave CPWs on porous Si

Measured and simulated quality factor of CPW1 and CPW2

Novel device topologies for RF and mm-waves

Slow wave concept, leading to slow-wave or shielded CPW TLlines
Implementation

**Technology stack**

S-CPW TL Technology

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Low-pass filters on porous Si

Low-pass filters using a combination of CPWs and S-CPWs on porous Si

Advantages:

High quality factor & wide range of characteristic impedances

Stepped-impedance low-pass filter
## Comparison between CPWs on different state-of-the-art substrates and porous Si

<table>
<thead>
<tr>
<th>Device</th>
<th>Description</th>
<th>Attenuation (dB/mm)</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPW</td>
<td>150um PoSi, 1um Al, p+ (0.001-0.005Ωcm)</td>
<td>0.33 @60GHz, 0.6 @110GHz</td>
<td>This work</td>
</tr>
<tr>
<td>CPW</td>
<td>1kΩcm HR-SOI 130nm SOI CMOS using HR Unibond Substrate by SOITEC</td>
<td>1.0 @110GHz</td>
<td>[3] (2006)</td>
</tr>
<tr>
<td>CPW</td>
<td>Cu M1-M6 (~5um) 130nm HR-SOI (SOITEC) Advanced CMOS (&gt;1kΩ.cm)</td>
<td>0.6 @60GHz, 1.3 @110GHz</td>
<td>[4] (2007)</td>
</tr>
<tr>
<td>CPW</td>
<td>Al 2.34μm on M6 S-lines 500nm Al on ground metal CMOS 0.18μm</td>
<td>0.73@60GHz</td>
<td>[2] (2011)</td>
</tr>
<tr>
<td>S-CPW</td>
<td>Al 3um on M6, Shield Cu 500nm on M1, BiCMOS-9MW 130nm ST</td>
<td>0.7 @110GHz</td>
<td>[1] (2012)</td>
</tr>
</tbody>
</table>

Ref. P. Sarafis, E. Hourdakis and A. G. Nassiopoulou, ESSDERC 2013
RF inductors on porous Si

1. $f_{\text{res}}$ shifted to higher values for inductors on PSi
2. The low permittivity of porous Si reduces crosstalk. Better than quartz


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Antennas on porous Si

Application in intra-chip communications
The EM wave is mainly guided into the substrate. Porous Si can be formed underneath the propagation layer to provide the necessary RF shielding from the bulk Si substrate.

Application in inter-chip communications
Advantage: Suppression of surface waves due to the low effective permittivity of PSi
Summary

- Porous Si local substrate: promising solution towards the digital/RF analog SoC on bulk Si
- High performance CPW TLines and inductors were realized on porous Si
- It allows for high characteristic impedance RF TLines on Si
- It reduces crosstalk between devices
- Porous Si constitutes an excellent solution to the on-chip integration of RF passives on bulk Si. It shows comparable/better performance than trap-rich HR SOI substrate. It is on bulk Si and of lower cost.
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- K. Ben Ali