Variability in Nanoscale CMOS and Nanowires

A. Asenov, A. R. Brown, G. Roy, A. Martinez, C. Alexander, M. F. Bukhori

University of Glasgow

www.elec.gla.ac.uk/groups/dev_mod
Summary

- Background
- Conventional CMOS
- Nanowire transistors
- Conclusions
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- Background
- Conventional CMOS
- Nanowire transistors
- Conclusions
Local statistical variability is a major source of concern

<table>
<thead>
<tr>
<th>Process</th>
<th>Environment</th>
<th>Temporal</th>
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<tbody>
<tr>
<td>(&lt;L_0&gt;) and (&lt;W&gt;)</td>
<td>T environment range</td>
<td>(&lt;\text{NBTI}&gt;)</td>
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<tr>
<td>(&lt;\text{layer thicknesses}&gt;)</td>
<td>(V_{dd}) range</td>
<td>Hot electron shifts</td>
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<td>Poly Si granularity</td>
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<td>High-k morphology</td>
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<td>Line width due to pattern density effects</td>
<td>Thermal hot spots due to non-uniform power dissipation</td>
<td>Computational load dependent hot spots</td>
</tr>
</tbody>
</table>

After D. J. Frank (IBM)
Statistical variability

Random dopants  Polysilicon/high-k Granularity  Line edge roughness
High-κ and metal gate morphology

- High-κ thickness of high κ
- Interfacial layer thickness
- Random grain orientation
- SiO₂
- HfO₂
- HfSiO
Glasgow statistical 3D simulation tools

- Drift-Diffusion (DD) with quantum corrections.
- Ensemble Monte Carlo (MC) with *ab-initio* impurity scattering.
- Non-Equilibrium Green’s Functions (NEGF).

Enabled by the power of cluster and grid computing
Summary

☐ Background
☐ Conventional CMOS
☐ Nanowire transistors
☐ Conclusions
Good agreement with measurements

<table>
<thead>
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<th>n-channel MOSFET</th>
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<th>p-channel MOSFET</th>
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<tr>
<td></td>
<td>$\sigma V_T$ [mV] (V$_{DS}$=0.05 V)</td>
<td>$\sigma V_T$ [mV] (V$_{DS}$=1.1 V)</td>
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<td>$\sigma V_T$ [mV] (V$_{DS}$=1.1 V)</td>
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<td>RDD</td>
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<td>LER</td>
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</table>
Combined variability in bulk MOSFETs

$t_{ox}$ scales according to ITRS

$t_{ox}$ remains constant

RD/D only
RD/D+LER/PSG (A)
RD/D+LER/PSG (B)

RD/D EOT from Table 1
RD/D EOT=1nm
Intel [23]
Transport (scattering) related variability

![Graph showing the relationship between gate length and transport variability](image)
The impact of the transport related variability

$V_D = 50 \text{ mV}$

$V_D = 1 \text{ V}$

35 nm MOSFET
Novel transistors are wanted mainly due to reduced statistical variability.

Assumption: Random dopant fluctuation is the main source of random variability. Line width roughness of Lg and Wg is not considered in this.
SOI and DG variability in NANOSIL testbed transistors

32 nm FD SOI

22 nm DG

$T_{ox} = 1.2$ nm

$T_{Si} = 7$ nm

$T_{ox} = 1.1$ nm

$T_{Si} = 10$ nm
### SOI and DG variability

**32 nm FD SOI**

![32 nm FD SOI Diagram](image)

**22 nm DG**

![22 nm DG Diagram](image)

<table>
<thead>
<tr>
<th></th>
<th>32nm $\sigma V_T$ (mV)</th>
<th>22nm $\sigma V_T$ (mV)</th>
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<tr>
<td></td>
<td>$V_{ds}$ (50mV)</td>
<td>$V_{ds}$ (1.0V)</td>
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<tr>
<td>RDD</td>
<td>5.3</td>
<td>6.1</td>
</tr>
<tr>
<td>LER</td>
<td>3.3</td>
<td>8.6</td>
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<tr>
<td>Trap (1e11)</td>
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<td>11</td>
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<td>Trap (5e11)</td>
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<td>Trap (1e12)</td>
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<tr>
<td>Combined (1e11)</td>
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<td>15</td>
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<tr>
<td>Combined (5e11)</td>
<td>25</td>
<td>27</td>
</tr>
<tr>
<td>Combined (1e12)</td>
<td>37</td>
<td>38</td>
</tr>
</tbody>
</table>
Statistical reliability: electrostatics

\[ \Delta V_T = \frac{\Delta Q}{C_{ox}} \]

\[ N_D = 1 \times 10^{11} \]
Threshold voltage variability increases with NBTI.

\[ N_t \text{ [cm}^{-2}\text{]} \]
- + 0
- \( 1 \times 10^{11} \)
- \( 5 \times 10^{11} \)
- \( 1 \times 10^{12} \)

Experiment

After V. Huard
The reason for ‘anomalously’ large threshold voltage shifts
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Single dopants in NEGF simulations

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Single dopants in NEGFL simulations

DD + DG Solution Potential

NEGFL solution
Electron density
Current density

Converged?

Yes
End

No

Nonlinear Poisson Solution
(auxiliary Fermi Level)
Single donor in the channel

Inverted sombrero potential

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Discrete donors in the source/drain

- Smooth
- Ra
- Ch
- Cr

$I_D$ [A] vs $V_G$ [V]

- $V_g=0\text{V}$
- $V_g=0.3\text{V}$
- $V_g=0.4\text{V}$

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Discrete donors in the source/drain

Classical S/D resistance 1.27 Ω
‘Quantum’ S/D resistance 1.13 Ω
Interface roughness

Surface roughness mobility 500 cm²/Vs
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Conclusions

- Statistical variability already becomes critical limitation to bulk MOSFET scaling.
- FD SOI and DG devices have significant advantages in terms of variability compared to bulk MOSFETs.
- Nanovire transistors are extremely susceptible to random dopants and interface roughness induced variability.