Tunnel FET or Ferroelectric FET to achieve a sub-60mV/decade switch

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Outline

• Power challenge in nanoelectronics
• Principles for small swing switches
• Tunnel FETs
  – Principle
  – State-of-the-art: experiments and simulations
  – Challenges and technology boosters
  – Sensitivity to technology parameters
• Negative capacitance FETs
  – Principle
  – Progress in the field
• Conclusions
The power challenge

- Power per chip continues increasing.
- Leakage power dominates in advanced technology nodes.
- $V_T$ scaling saturated by 60mV/dec physical limit.
- Voltage scaling slowed (90nm: 1.2V, 45nm: 1V, 22nm: 0.8V)

Power challenge due to $kT/q=60\text{mV/dec}$ limit at RT

Reducing threshold voltage 
by 60mV 
increases the leakage current (power) 
by ~10 times

See also: C. Hu @ INC 2009, UCLA.
Why 60mV/dec limit?

- carrier injection by lowering the barrier
- subthreshold current is a diffusion current

\[ I_D = q \frac{W}{L} \left( \frac{n_i^2}{N_A} \right) \left( \frac{k_B T}{q} \right)^2 \frac{\mu_{\text{eff}} e^{QV_{GS}/m k_B T}}{E_S} \left( 1 - e^{-qV_{DS}/k_B T} \right) A \]

\[ m = 1 + \frac{C_D}{C_{OX}} \]

\[ SS = \frac{dV_g}{d(\log_{10} I_d)} = \ln 10 \frac{kT}{q} \left( 1 + \frac{C_{\text{dep}}}{C_{ox}} + \frac{C_{ss}}{C_{ox}} \right) \]

\[ \rightarrow \frac{kT}{q} \ln 10 = 60mV / \text{decade} \quad @ \text{RT} \]

Power challenge: rescue strategies

- new **software-hardware techniques** from system to circuit level dedicated to power savings

- the identification of novel power aware or energy efficient device architectures: **small swing switches**
Parallelism to the rescue

CMOS has a fundamental lower limit in energy per operation due to subthreshold leakage

Parallelism (multi-core) is a key technique to improve system performance under a power budget

\[ E_{\text{dynamic}} + E_{\text{leakage}} = \alpha L_d C V_{dd}^2 + L_d I_{\text{off}} V_{dd} t_{\text{delay}} \]

Source: T.J. King, UC Berkeley.
Strategy for digital switches

• **Goal**
  
  $V_{dd} = 0.2V \rightarrow \text{Leakage power reduced by 100}$

• **How?**
  
  – Channel engineering to reduce the $V_{dd} - V_t$ (Ge, III-V, graphene, etc).
  
  – Nanowire and nanotube FETs for improved electrostatic (subthreshold leakage) control.
  
  – Operate circuits at low (cryogenic) temperatures.
  
  – **Reduce the threshold voltage by achieving a small swing switch: novel devices.**
55nm CMOS to beat

Numbers to beat:

\[ \frac{I_{on}}{I_{on}} = \frac{780}{400} \mu A/\mu m \]

\[ I_{off} = 3nA/\mu m \]

\[ \frac{I_{on}}{I_{off}} = 2.6 \times 10^5 @ 1.2V \]

NEC @ VLSI 2006
Nanowires to the rescue

- NW MOSFET: better electrostatic control, lower I_{off}
- L\sim 0.35\mu m, NW diameter \sim 30nm
- I_{on}/I_{off} <10^6, S \sim 62–75 mV/dec and low DIBL (20mV/V)
- I_{off} savings compared to bulk CMOS is \sim 10 times
- Current per NW: \sim 1\mu A \rightarrow arrays needed!

The quasi-ideal switch

A quasi-ideal nanoelectronic switch has **ZERO standby power** and offers all wanted on current. It should be very fast.

- **Quasi-ideal binary switch, what matters:**
  - 2 stable states (off, on)
  - Ion: as high as possible
  - loff: as low as possible
  - Ion/loff > $10^5$
  - abrupt swing (mV/decade)
  - very fast (<ns)
Sub-kT/q subthreshold slope switch to the rescue

- MOSFET is a vampire switch at nanoscale
- New Small Swing Switch = New physics
- SSS: low standby power switch

MOSFET Switch: SS~60mV/dec @ RT

Small Swing Switch
Principles for SS < 60mV/decade

\[ S = \frac{\partial V_g}{\partial (\log I_d)} = \frac{\partial V_g}{\partial \psi_S} \frac{\partial \psi_S}{\partial (\log I_D)} = \left(1 + \frac{C_s}{C_{ins}}\right) \frac{kT}{q} \ln 10 \]

- \( m \) less than 1
  - NEM relay or FET
  - positive feedback gate material (Fe-FET)
  - Other ideas?

- \( n \) less than \((kT/q)\ln 10\)
  - Tunnel FETs
  - Impact Ionization
  - Other ideas?
Tunnel FETs
Tunnel FET: principle (1)

**OFF-state**
- $V_d = \text{positive}$
- $V_g = 0$
- no current flows

**ON-state**
- $V_d = \text{positive}$
- $V_g = \text{positive}$
- barrier thin, current flows
Tunnel FET: principle (2)

- Barrier control: key for Tunnel FET operation

All-silicon DG Tunnel FET

- gate dielectric (thickness, permittivity)
- silicon film thickness (UTB, NW)
- bandgap
- fringing fields (gate alignment to the junction)
Tunnel FET: principle (3)

\[ I = A V_{\text{eff}} \xi \cdot \exp\left(-\frac{B}{\xi}\right) \]

\[ S = \left( d \log I_d / dV_{gs} \right)^{-1} \]

\[ = \ln 10 \left( \frac{1}{V_{\text{eff}}} \frac{dV_{\text{eff}}}{dV_{gs}} + \frac{\xi + B}{\xi^2} \frac{d\xi}{dV_{gs}} \right)^{-1} \]

- \( S \) is gate bias dependent: lower @ lower \( V_{GS} \)
- \( B_{\text{Kane}} \) depends on effective mass
- \( D \) depends on \( \text{tox}, \text{L}, \text{Vds}, \text{dopings} \)

\[ S \bigg|_{V_{GS} \to 0} \to 0 \]

Point swing < 60mV/dec / ln10 = 26mV/dec @ RT

What about average swing?
First experimental demonstration: 40mV/dec in CNT Tunnel FETs

- dissipative quantum transport simulations of CNT FETs using the non-equilibrium Green’s function (NEGF) formalism.

M. Lundstrom

On-current: ~1µA/tube

UC Berkeley: experimental 53mV/dec silicon Tunnel FETs

- Ion=12µA/µm, Ioff=5.4nA/µm
- S small in a very limited range
- large drain-to-gate leakage
- Ion/Ioff less than for MOSFET

IEEE EDL 2007, UC Berkeley.
MIT staggered heterojunction Tunnel FETs

- Tunneling Field-Effect Transistors using **Strained Silicon/Strained-Germanium Type-II staggered heterojunctions**

![Simulated HTFET](image)

Fig. 4. Simulated (a) transfer and (b) output characteristics for the HTFET shown in (solid lines) Fig. 1(a) and (dashed lines) a 22-nm node n-MOSFET with $SS = 80$ mV/dec and DIBL = 100 mV/V. Both devices have $EOT = 1$ nm. The gate workfunction of the HTFET device is 4.4 eV.

Heterojunction Tunnel FETs: staggered versus broken band line-up

- High on state performance predicted
- minimal $S$ value in the case of staggered band line-up

Stanford: Experimental $I_{on}=300\mu A/\mu m$ in Ge Tunnel FET

DG TFET with **strained Ge heterostructure channel**:

- high drive currents ($I_{on}\sim300\mu A/\mu m$) for $V_d=3V$
- **But** the low $SS\sim50mV/\text{dec}$, due to small bandgap of $s$-Ge and DG electrostatics and $I_{off}$ are for $V_d=0.5V$.

IMEC’s Ge/SiGe-source vertical Tunnel FET

- Smaller bandgap $\rightarrow$ improved tunneling but $I_{off}$ high

LETI’s experimental Tunnel FETs

**GeOI versus SOI Tunnel FETs**

- **Graph 1:**
  - Drain current $I_D$ vs. $V_{GS} - V_{BtBt}$ and $V_{GD} - V_{BtBt}$
  - $t_{SiGe} = t_{Si} = 20\text{nm}$
  - $L_G = 400\text{nm}$
  - $x_{Ge} = 15\%$ (GeOI), $x_{Ge} = 30\%$ (GeOI), $x_{Si} = 30\%$ (SOI)

- **Graph 2:**
  - Drain current $I_D$ vs. $V_{GS}$ and $V_{GD}$
  - $V_{DG}$: $0.1/0.2/0.4$ $\text{V}$
  - $V_{BST}$: $-0.1/0.2/0.4$ $\text{V}$
  - $S = 42$ $\text{mV/dec}$

IBM bottom-up NW Tunnel FETs

VLS grown Si NWs tunnel FETs with different gate stacks (SiO$_2$ and HfO$_2$); the use of a high-k gate dielectric markedly improves the TFET performance in terms of average slope and on-current.

Ion~0.3uA/um, Ion/Ioff ~10$^5$

20nm Tunnel FET versus CMOS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MOSFET\textsuperscript{a}</th>
<th>Tunnel transistor</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>2007</td>
<td>2010</td>
<td>2013\textsuperscript{b}</td>
</tr>
<tr>
<td>Gate length $L_G$</td>
<td>25</td>
<td>18</td>
<td>13</td>
</tr>
<tr>
<td>Gate width $W \sim 10L_G$</td>
<td>250</td>
<td>180</td>
<td>130</td>
</tr>
<tr>
<td>Equivalent oxide thickness EOT</td>
<td>1.1</td>
<td>0.65</td>
<td>0.5</td>
</tr>
<tr>
<td>Supply voltage $V_{DD}$</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
</tr>
<tr>
<td>On current $I_{ON}$</td>
<td>428</td>
<td>701</td>
<td>1053</td>
</tr>
<tr>
<td>Off current $I_{OFF}$</td>
<td>0.29</td>
<td>2.02</td>
<td>1.88</td>
</tr>
<tr>
<td>Oxide capacitance density $C_{OX} \sim \varepsilon_{Si}/\varepsilon_{OX}$</td>
<td>31.4</td>
<td>53.1</td>
<td>69.1</td>
</tr>
<tr>
<td>Gate capacitance $C_G \sim C_{OX}L_G$</td>
<td>0.78</td>
<td>0.96</td>
<td>0.90</td>
</tr>
<tr>
<td>Intrinsic speed $\gamma \sim C_{VDD}/I_{ON}$</td>
<td>0.92</td>
<td>0.68</td>
<td>0.43</td>
</tr>
<tr>
<td>Leakage $P_{leak} \sim nI_{leak}V_{DD}$</td>
<td>7.25</td>
<td>50.50</td>
<td>47.00</td>
</tr>
<tr>
<td>Dynamic $P_{dyn} \sim 1/2nI_{ON}V_{DD}^2\alpha$</td>
<td>107</td>
<td>175</td>
<td>263</td>
</tr>
<tr>
<td>Total $P \sim P_{leak} + P_{dyn}$</td>
<td>114</td>
<td>226</td>
<td>310</td>
</tr>
<tr>
<td>Leakage $E_{leak} \sim (nI_{leak})V_{DD}(nc)$</td>
<td>332</td>
<td>1722</td>
<td>1002</td>
</tr>
<tr>
<td>Dynamic $E_{dyn} \sim 1/2(nC_{VDD})V_{DD}^2\alpha$</td>
<td>98</td>
<td>120</td>
<td>112</td>
</tr>
<tr>
<td>Total $E \sim E_{leak} + E_{dyn}$</td>
<td>430</td>
<td>1842</td>
<td>1114</td>
</tr>
</tbody>
</table>


- Solution: heterostructure transistor
- What about all-silicon Tunnel FET?
Simulation: all-Si Double Gate Tunnel FET with high-k dielectric

Sub-1V all-silicon Tunnel FET

- **Additive technology boosters**

  \[ I_{on} \approx 1\text{mA/\mu m} \]
  \[ I_{on}/I_{off} > 10^{10} \]

  A) Single gate SOI, \( L=100\text{nm}, 3\text{nm SiO}_2 \)
  B) stress = 4 GPa at source junction
  C) high-K gate dielectric
  D) double gate
  E) oxide aligned to \( i \)-region
  F) \( L=30\text{nm} \)

1V all-silicon asymmetrically strained Tunnel FET

Boosters
A+B+C+D
- Avg SS ~ 50mV/dec
- Point SS ~15mV/dec
- $V_D=V_G=1V$
- Very low $V_{TD}$

$V_{TG}$ reduced from 1.5 V
-> 0.5 V

Silicon Tunnel FET: energy performance comparison

- For high-performance applications requiring $I_{on} > 100uA/um$, TFET has a larger average subthreshold slope $S$ value and hence would consume more energy than a MOSFET: $S_{avg}$ very important.
- TFET seems better in energy efficiency for applications $<1GHz$.
- TFET variability should be addressed.

Energy and performance: Tunnel FETs versus FinFET & PD SOI

D.J. Frank, IBM, Node Workshop, Zurich, 2009.
Negative capacitance FET
Negative capacitance FET (NC-FET)

- step-up voltage transformer that could amplify the gate voltage, thus leading to values of $S$ lower than 60mV/dec possible in ferroelectric gate-stack FET (Sallahudin & Datta)

Possible to find such insulator and stabilize it?
Ferroelectric gate stack NC-FET

- Simulation with ferroelectric in the negative capacitance region; the subthreshold swing improves significantly, which unexpected from a typical high-k dielectric.

Organic ferroelectric gate stack FET

- 40nm PVDF / 10nm SiO$_2$ gate stack FET shows atypically low SS @ low currents.
- Due to stabilized negative capacitance? More experimental proof needed. Artifact of leakage?

PVDF gate stack on SOI MOSFET
Unique SS(T) in PVDF Fe-FET

- In Fe-FETs subthreshold swing appears to decrease with T, in contrast with traditional MOSFET

\[
SS = \frac{\partial V_g}{\partial (\log I_d)} = \frac{\partial V_g}{\partial \psi_S} \frac{\partial \psi_S}{\partial (\log_{10} I_D)} = (1 + \frac{C_s}{C_{ox}C_{Ferro}}) \frac{k_B T}{q} \ln 10
\]

\[
C_s(T) = C_s \\
C_{ox}(T) = C_{ox} \\
C_{Ferro} = \frac{1}{\alpha(T - T_0)} \frac{1}{d}
\]

G. Salvatore et al, ESSDERC 2009.
Conclusions

Main challenges

Tunnel FET (non-hysteretic)
- improve Ion
- tunnel junction engineering
- implementation on silicon platforms

Fe-FET (hysteretic?)
- experimental proof of concept
- identification of most suited gate stack materials
- Full theory to be developed

Experimentally demonstrated
Needs further experimental proof
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